ST.ANNE'S

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi. Affiliated to Anna University, Chennai)
(An ISO 9001: 2015 Certified Institution) ANGUCHETTYPALAYAM,
PANRUTI – 607 106.

.

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

LAB MANUAL

JAN 2023– MAY 2023 / EVEN SEMESTER

SUBJECT CODE/NAME:

EE3412/ LINEAR AND DIGITAL INTEGRATED CIRCUITS LABORATORY

YEAR/SEM: II/IV **BATCH**: 2021- 2025

AS PER ANNA UNIVERSITY, CHENNAI REGULATION 2021

LIST OF EXPERIMENTS

1. Implementation of Boolean Functions, Adder and Subtractor circuits.

2. Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa

3. Parity generator and parity checking

4. Encoders and Decoders

5. Counters: Design and implementation of 3-bit modulo counters as synchronous and Asynchronous types using FF IC's and specific counter IC.

6. Shift Registers: Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO modes using suitability IC's.

7. Study of multiplexer and de multiplexer

8. Timer IC application: Study of NE/SE 555 timer in Astability, Monostability operation.

9. Application of Op-Amp: inverting and non-inverting amplifier, Adder, comparator, Integrator and Differentiator.

10. Voltage to frequency characteristics of NE/ SE 566 IC.

11. Variability Voltage Regulator using IC LM317.

Ex. No. 1 Date:	IMPLEMENTATION OF BOOLEAN FUNCTIONS, ADDER / SUBTRACTOR CIRCUITS

INTRODUCTION:

HALF ADDER:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables
produce the sum and carry bits.

FULL ADDER:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

HALF SUBTRACTOR:

A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

FULL SUBTRACTOR:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

ANNA UNIVERSITY QUESTIONS

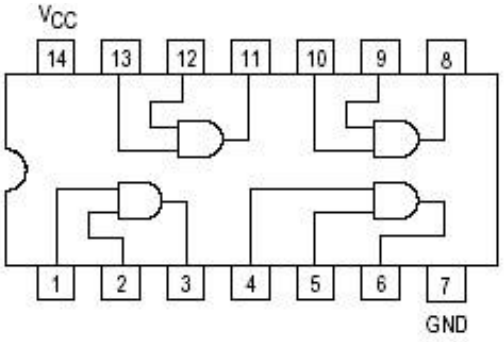
1. Design and verify the truth table of a circuit which implements the following Boolean function F(A,B,C,D)=∑m =(0,1,2,4,5,7,9,12,14) using logic gates. (100)
2. Simplify using K-map and implement using any suitable logic gates
   F (A,B,C,D) = Σ (3,4,5,7,9,13,14,15) (100)
3. Design and construct a half subtractor and full subtractor by using suitable logic gated and verify its truth table. (100)
4. Design and construct a half adder and full adder by using suitable logic gated and
   verify its truth table.
   (100)

AIM:

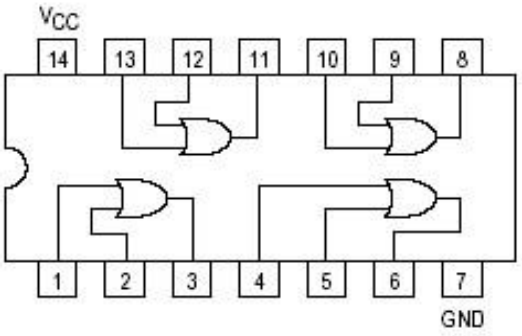
(a) To minimize Boolean functions using K-map and to implement the same in POS and SOP forms using basic gates.

(b) To design and verify the truth table of the Adder & Subtractor circuits.

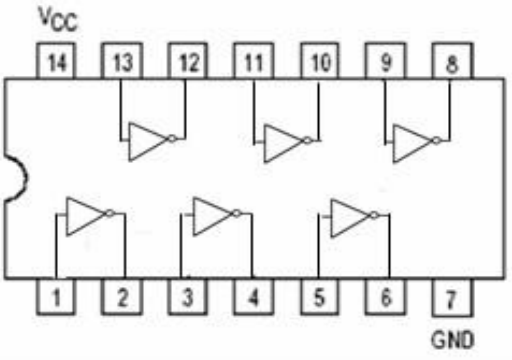
PIN DIAGRAM OF IC 7408:



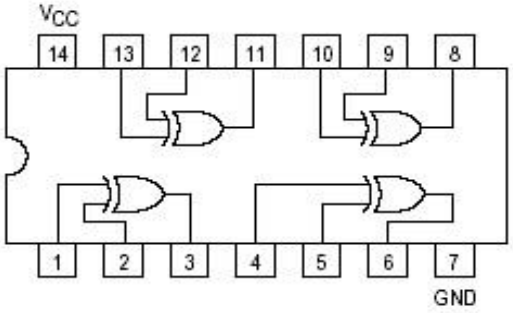
PIN DIAGRAM OF IC 7432:



PIN DIAGRAM OF IC 7404:



PIN DIAGRAM OF IC 7486:



PRE-LAB QUESTIONS:

1. In Boolean algebra the AND function is represented by the '+' sign

   a). True b). False

2. What is the most widely used method for the automated simplification of Boolean expressions?

   a). Fast Fourier transforms b). Quine-McCluskey minimisation

   c). Binary reduction d). Karnaugh maps

3. Physical logic gates take a finite time to respond to changes in their input signals.

   What name is given to this time?

   a). Propagation delay time b). Rise time

   c). Hold time d). Set-up time

4. Express the binary number 1001 in decimal

   a). 9 b). 11

   c). 13 d). 15

5. Which of the following expressions is in the sum-of-products (SOP) form?

   a). (A + B)(C + D) b). (A)B (CD)

   c). AB (CD) d). AB + CD

APPARATUS REQUIRED:

Sl.No	Component	Specification	Quantity
1	AND GATE	IC 7408	1
2	X-OR GATE	IC 7486	1
3	NOT GATE	IC 7404	1
4	OR GATE	IC 7432	1
5	IC TRAINER KIT	-	1
6	PATCH CORDS	-	As required

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the IC's 7^{th} pin is grounded and 14^{th} pin is connected to +5 V supply (V_{CC}).
3. Apply the inputs and verify the truth table for the respective logic circuits.

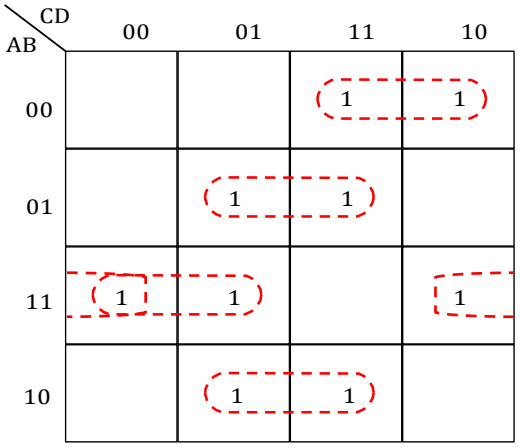
i. MINIMIZATION OF BOOLEAN FUNCTION IN SOP

TRUTH TABLE – SOP:

Input				Output
A	**B**	**C**	**D**	**F**
0	0	0	0	**0**
0	0	0	1	**0**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**0**
0	1	1	1	**1**
1	0	0	0	**0**
1	0	0	1	**1**
1	0	1	0	**0**
1	0	1	1	**1**
1	1	0	0	**1**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**0**

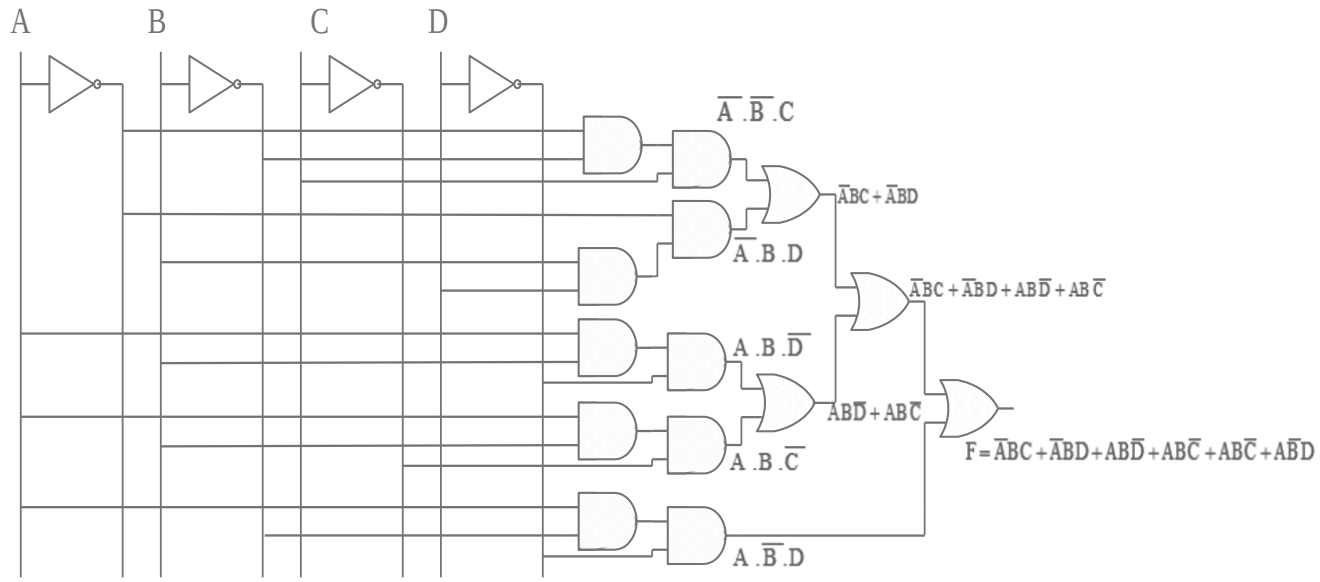
SUM OF PRODUCTS:

F= ∑m (2, 3, 5, 7, 9, 11, 12, 13, 14)



$$F = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}D + A\bar{B}\bar{C} + ABD$$

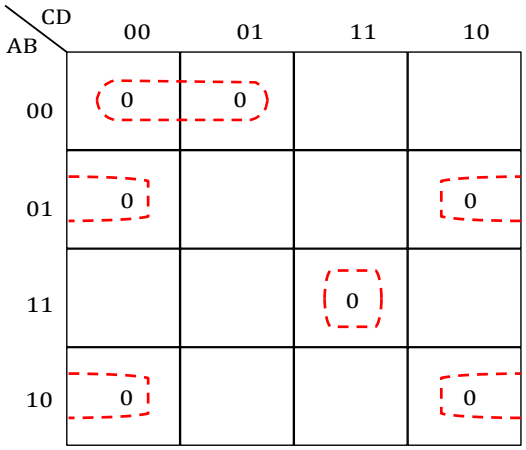
LOGIC DIAGRAM – SOP:



ii. PRODUCT OF SUMS:

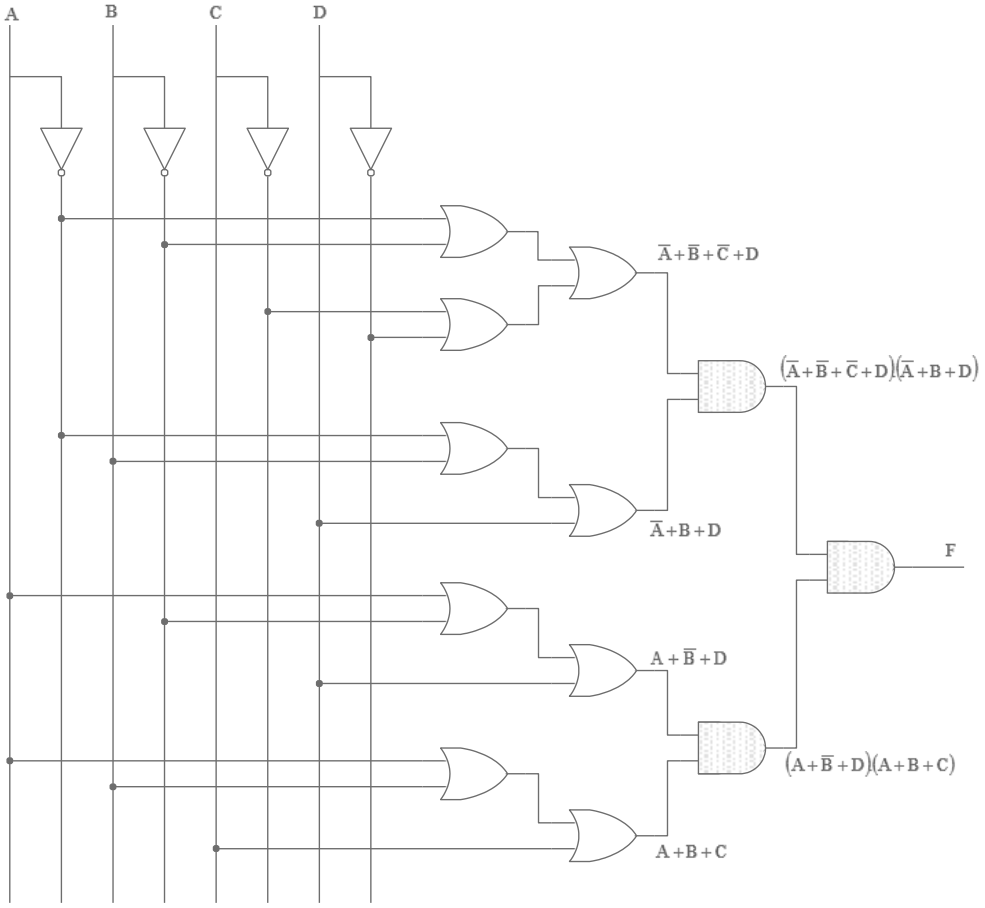
TRUTH TABLE – POS:

Inputs				**Outputs**
A	**B**	**C**	**D**	**F**
0	0	0	0	**0**
0	0	0	1	**0**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**0**
0	1	1	1	**1**
1	0	0	0	**0**
1	0	0	1	**1**
1	0	1	0	**0**
1	0	1	1	**1**
1	1	0	0	**1**
1	1	0	1	**1**
1	1	1	0	**1**
1	1	1	1	**0**



F = (A + B + C)(A + B + D)(A + B + C + D)(A + B + D)

LOGIC DIAGRAM – POS:



IMPLEMENTATION OF HALF ADDER, FULL ADDER, HALF SUBTRACTOR AND FULL SUBTRACTOR CIRCUITS:

HALF ADDER:

TRUTH TABLE:

Inputs		Output	
A	**B**	**Sum**	**Carry**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

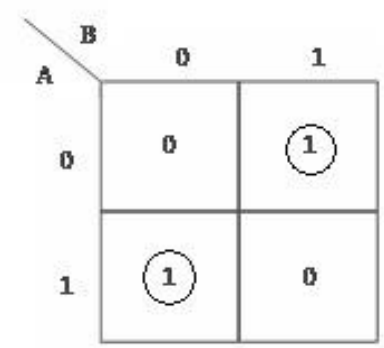
DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as,

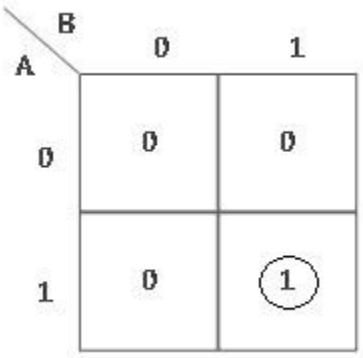
Sum, $S = A \oplus B$

Carry, $C = A \cdot B$

SUM:



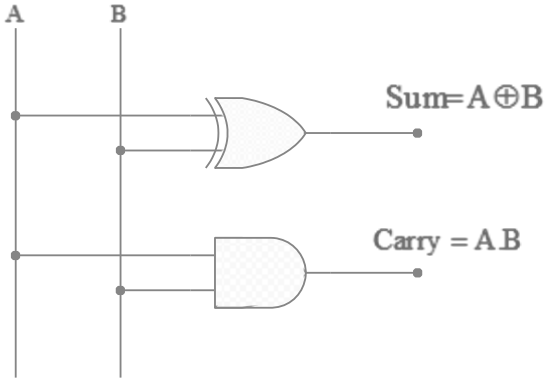
CARRY:



Sum = $(A.\overline{B} \cdot \overline{A}B) \cdot A \cdot B$

Carry = A.B

LOGIC DIAGRAM OF HALF ADDER:



FULL ADDER:
TRUTH TABLE:

Inputs			Output	
A	**B**	**C**	**Sum**	**Carry**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

DESIGN:

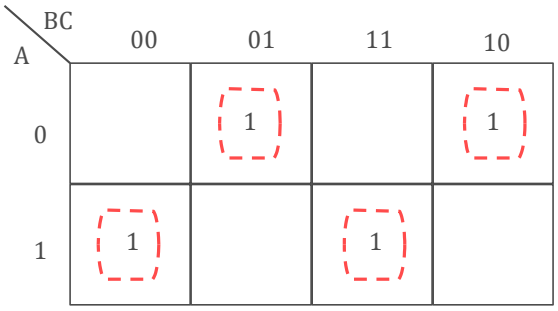
From the truth table the expression for sum and carry bits of the output can be obtained as,

SUM = A’B’C + A’BC’ + AB’C’ + ABC

CARRY = A’BC + AB’C + ABC’ +ABC

Using Karnaugh maps the reduced expression for the output bits can be obtained as,

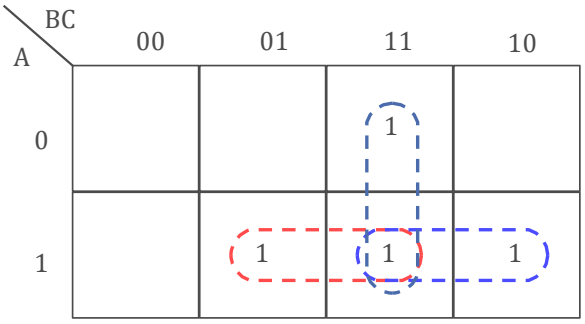
SUM



Sum = $(\overline{A}.\overline{B}.C + A.\overline{B}.\overline{C} + A.\overline{B}.C + A.B.C)$

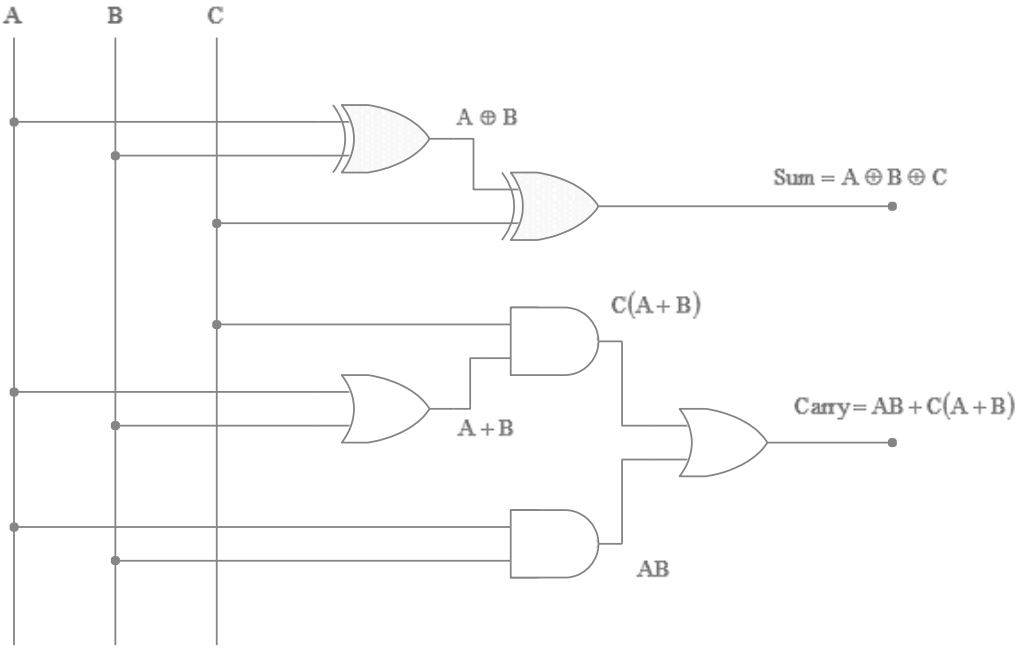
$\cdot A \cdot B \cdot C$

CARRY



CARRY = AB + AC + BC

LOGIC DIAGRAM OF FULL ADDER:



HALF SUBTRACTOR:

TRUTH TABLE:

Inputs		Output	
A	**B**	**Difference**	**Borrow**
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

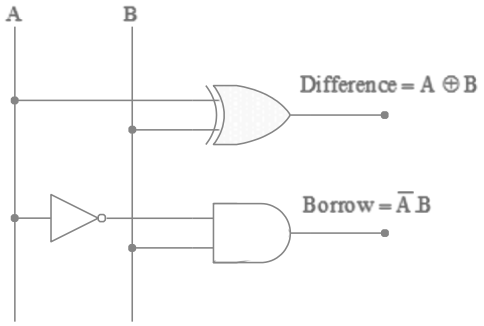
DESIGN:

From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference, DIFF = A $\oplus$ B

Borrow, BORR = A'. B

LOGIC DIAGRAM OF HALF SUBTRACTOR:



FULL SUBTRACTOR:

TRUTH TABLE:

Inputs			Output	
A	**B**	**C**	**Difference**	**Borrow**
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

DESIGN:

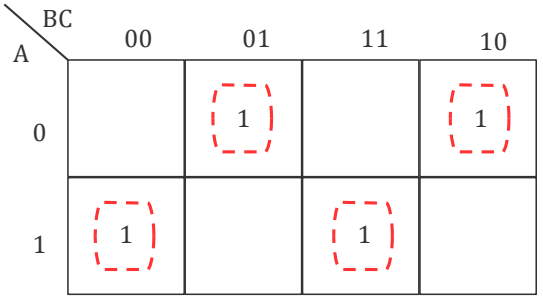
From the truth table the expression for difference and borrow bits of the output can be obtained as,

Difference= A’B’C + A’BC’ + AB’C’ + ABC

Borrow = A’BC + AB’C + ABC’ +ABC

Using Karnaugh maps the reduced expression for the output bits can be obtained as,

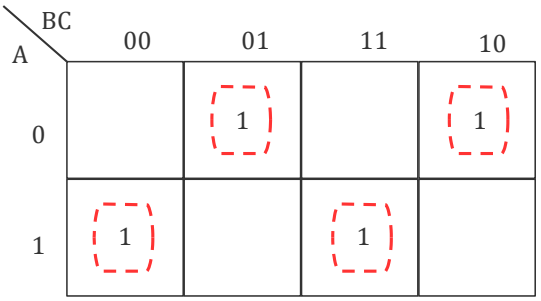
DIFFERENCE



DIFFERENCE = $(\bar{A}.\bar{B}.C + A.\bar{B}.\bar{C} + \bar{A}.B.\bar{C} + A.B.C)$

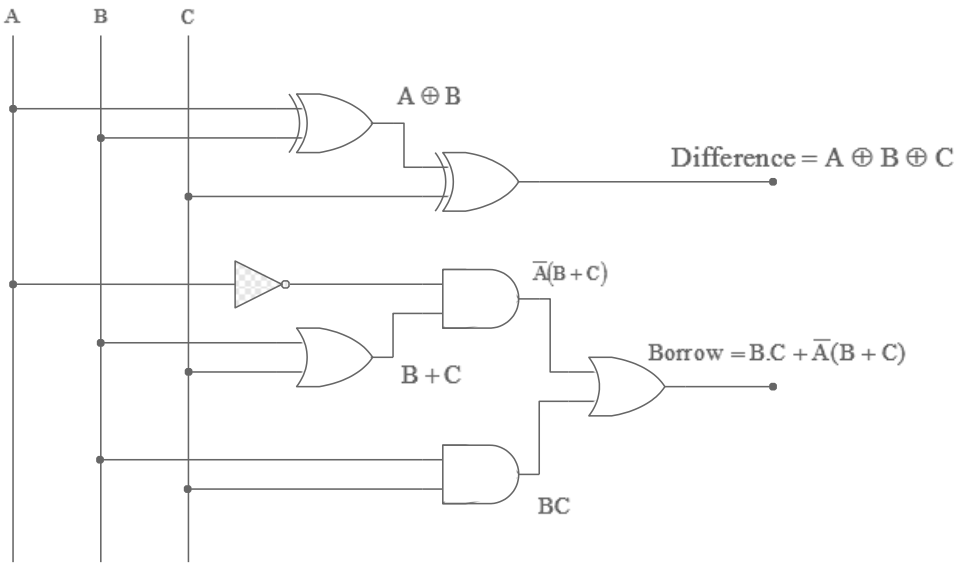
$= A.B.C$

BORROW



BORROW $= B.C + \bar{A}(B + C)$

LOGIC DIAGRAM OF FULL SUBTRACTOR:



VIVA QUESTIONS:

1. What are the associative laws of Boolean algebra?
2. Why NAND and NOR are called Universal Gates?
3. What is meant by sum of product form?
4. What is the use of a full adder circuit?
5. What is a subtractor?

POST-LAB QUESTIONS:

1. Half-adders can be combined to form a full-adder with no additional gates.

   a). True b). False

2. A full-adder adds _____.

   a). two single bits and one carry bit b). two 2-bit binary numbers

   c). two 4-bit binary numbers d). two 2-bit numbers and one carry bit

3. Use Boolean algebra to find the most simplified SOP expression for F = ABD + CD + ACD + ABC + ABCD.

   a). F = ABD + ABC + CD b). F = CD + AD

   c). F = BC + AB d). F = AC + AD

4. Fast-look-ahead carry circuits found in most 4-bit full-adder circuits:

   a). determine sign and magnitude b). Reduce propagation delay

   c). add a 1 to complemented inputs d). Increase ripple delay

5. Why is a fast-look-ahead carry circuit used in the 7483 4-bit full-adder?

   a). to decrease the cost b). To make it smaller

   c). to slow down the circuit d). To speed up the circuit

RESULT:

(a) The minimization of Boolean functions using K-map is performed and same is

implemented in POS and SOP forms using basic gates.

(b) The design of the Adder and Subtractor circuits was done and the corresponding truth tables were verified.

Ex. No. 2	CODE CONVERTERS
Date:	

INTRODUCTION:

Code converter is a circuit that makes two systems compatible even though each uses different binary codes. There is a wide variety of binary codes used in digital systems. Some of these codes are Binary Coded Decimal, Gray code, Excess- 3 code , ASCII code, etc.

ANNA UNIVERSITY QUESTIONS

1. Design a 3 bit binary to gray code converter and verify its truth table. (50)
2. Design a gray to binary code converter using suitable logic gates and verify their function. (50)
3. Design and construct binary to gray code converter and gray to binary code converter by using suitable logic gated and verify its truth table. (100)
4. Design and construct BCD to Excess-3code converter by using suitable logic gated and verify its truth table. (100)
5. Design and construct Excess-3 to BCD code converter by using suitable logic gated and verify its truth table. (100)

AIM:

To construct logic diagram and to verify the truth table for,

(a) Excess-3 to BCD code converter

(b) BCD to Excess-3 code converter

(c) Binary to Gray code Converter

(d) Gray to Binary code converter

EXCESS -3 TO BCD CONVERTER:

TRUTH TABLE:

Excess – 3 input				**BCD output**			
A	**B**	**C**	**D**	**B3**	**B2**	**B1**	**B0**
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

PRE-LAB QUESTIONS

1. How many outputs are on a BCD decoder?

   a). 4 b). 16

   c). 8 d). 10

2. The expansion inputs to a comparator are used for expansion to a(n):

   a). 4-bit system b). 8-bit system

   c). BCD system d).Counter system

3. A BCD decoder will have how many rows in its truth table?

   a). 10 b). 9

   c). 8 d). 3

4. A binary code that progresses such that only one bit changes between two successive codes is:

   a). nine's-complement code b). 8421 code

   c). excess-3 code d). Gray code

5. Which type of error is eliminated through the use of the Gray code?

   a). decoding b). timing

   c). encoding d). conversion

APPARATUS REQUIRED:

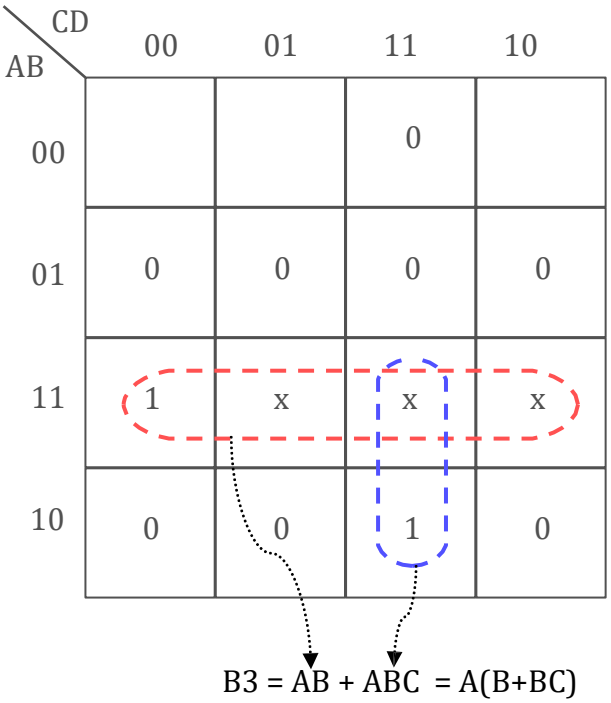
Sl.No	Component	Specification	Quantity
1	AND GATE	IC 7408	1
2	X-OR GATE	IC 7486	1
3	NOT GATE	IC 7404	1
4	OR GATE	IC 7432	1
5	IC TRAINER KIT	-	1
6	PATCH CORDS	-	As required

PROCEDURE:

- The logic circuit is designed using K map.
- Gates are decided for the logic circuit.
- Connections are made as per the logic diagrams.
- Truth tables are verified.

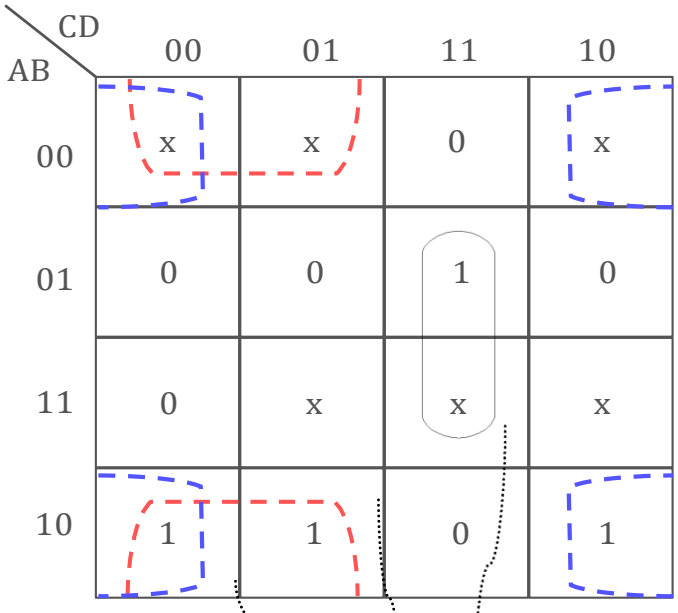
K- MAP: **EXCESS – 3 TO BCD**

B3:



B3 = AB + ABC = A(B+BC)

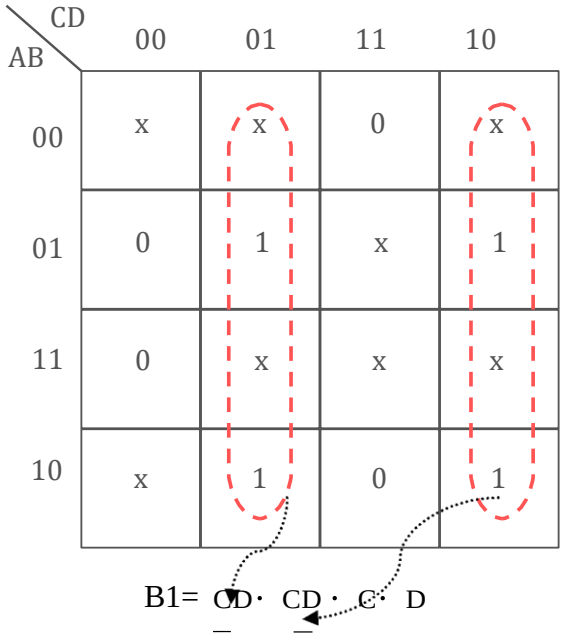
B2:



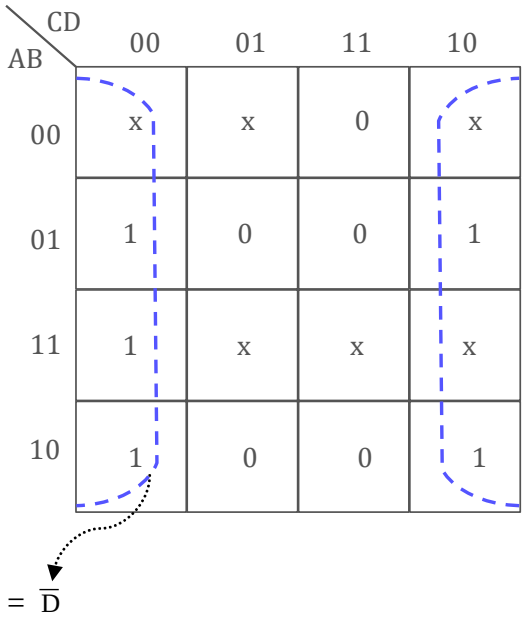
B2 = $\overline{B}\overline{D} \cdot \overline{B}\overline{C} \cdot BCD$

B2 = $\overline{B(C \cdot D)} \cdot BCD$ $= B \cdot \overline{C \cdot D}'$

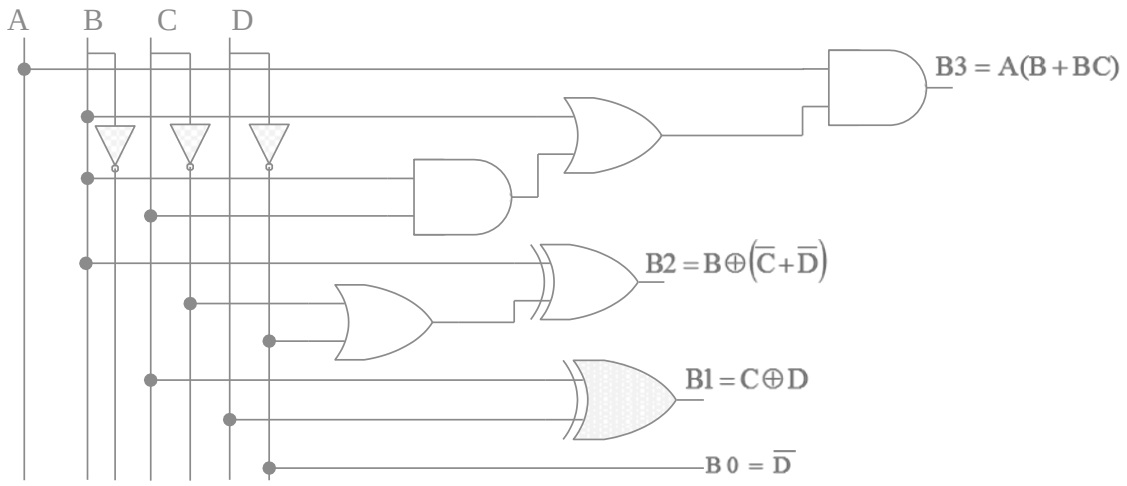
B1:


CD
AB
00
01
11
10
x x 0 x
0 1 x 1
0 x x x
x 1 0 1
B1= CD · CD · C · D

B0:


CD
AB
00
01
11
10
x x 0 x
1 0 0 1
1 x x x
1 0 0 1
B0 = D

LOGIC DIAGRAM OF EXCESS – 3 TO BCD CONVERSION

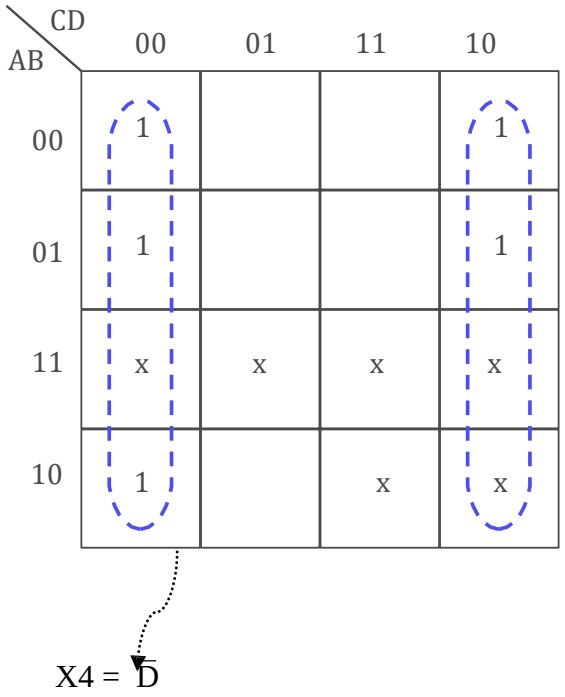


BCD TO EXCESS -3 CONVERTER:

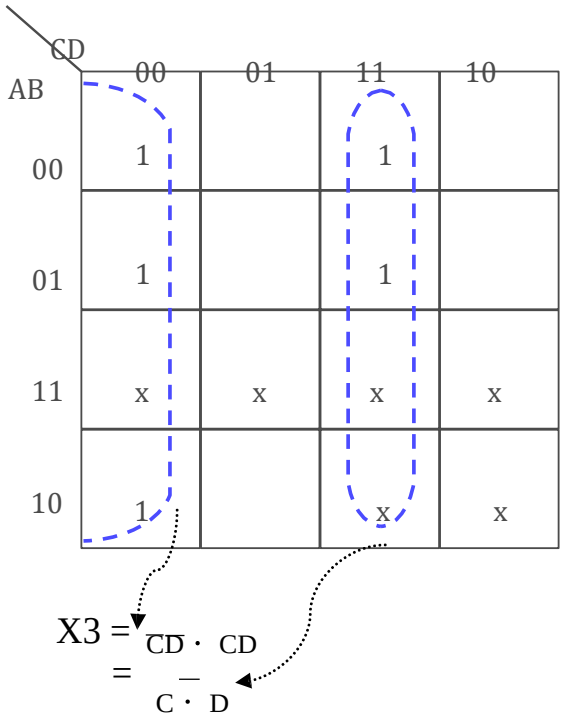
TRUTH TABLE:

BCD input				**Excess – 3 output**			
A	**B**	**C**	**D**	**X1**	**X2**	**X3**	**X4**
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x

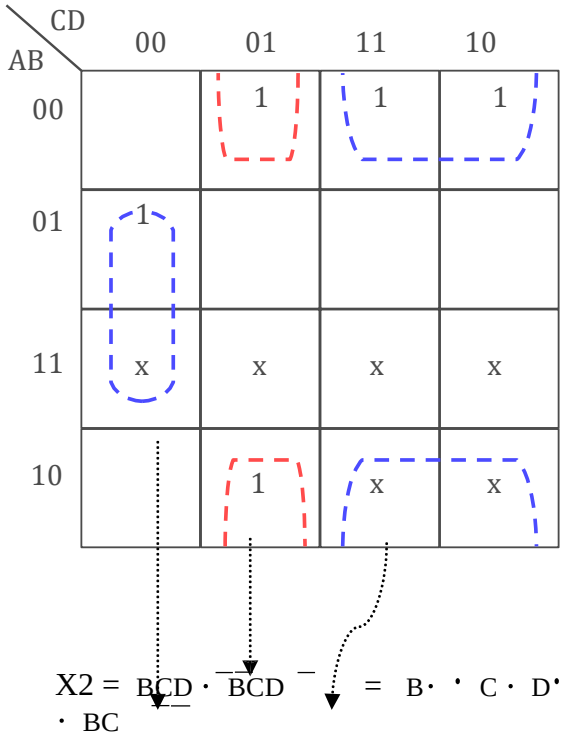
X4:


CD
AB
00
01
11
10
1
1
1
1
1
1
x
x
x
x
1
x
x
X4 = D

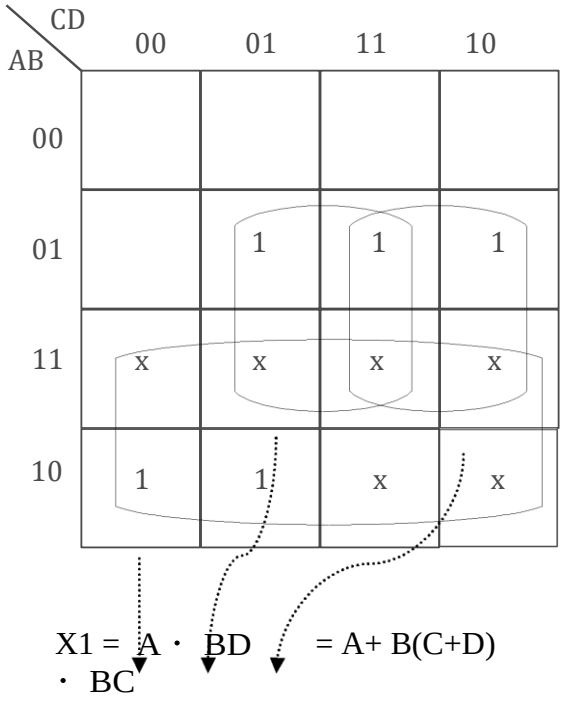
X3:


CD
AB
00
01
11
10
1
1
1
1
1
1
x
x
x
x
1
x
x
X3 = CD · CD
= C · D

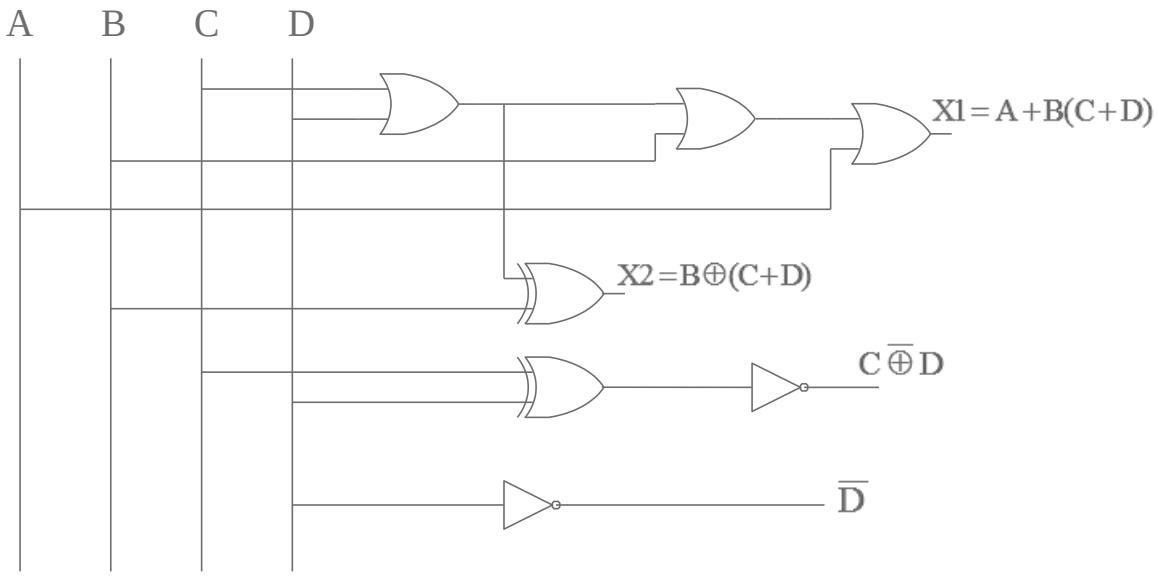
X2:


CD
AB
00
01
11
10
00
01
11
10
1
1
1
1
x
x
x
x
1
x
x
X2 = BCD · BCD = B · · C · D · BC

X1:


CD
AB
00
01
11
10
00
01
11
10
1
1
1
x
x
x
x
1
1
x
x
X1 = A · BD = A+ B(C+D)
· BC

LOGIC DIAGRAM:



BINARY TO GRAY CODE CONVERTER

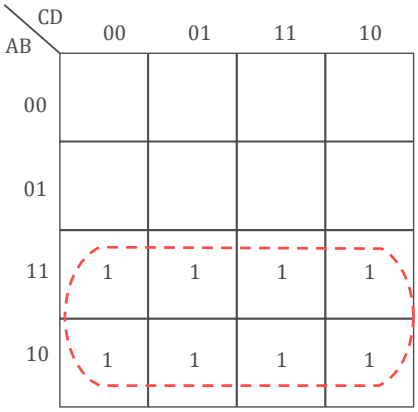
TRUTH TABLE:

BINARY CODE				**GRAY CODE**			
A	**B**	**C**	**D**	**G1**	**G2**	**G3**	**G4**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0

1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

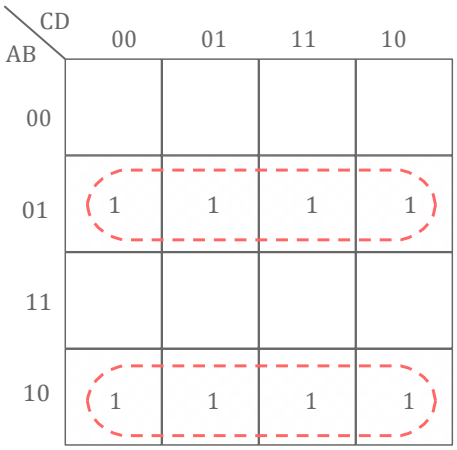
K- MAP: **BINARY TO GRAY**

G1:



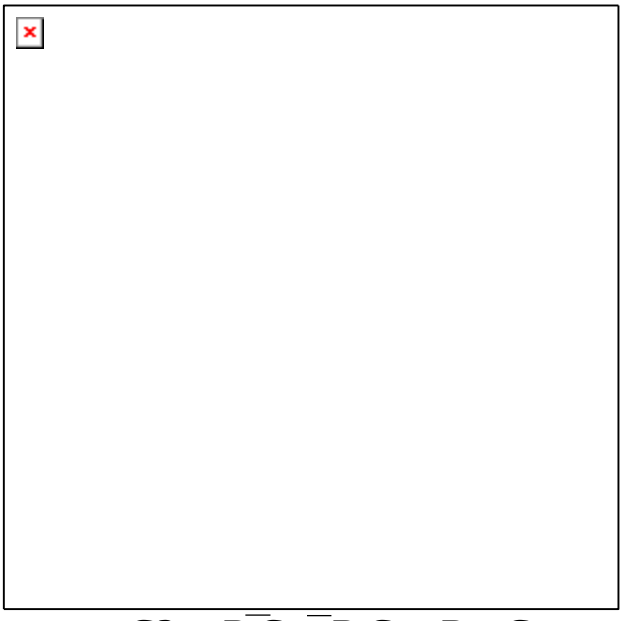
G1 = A

G2:



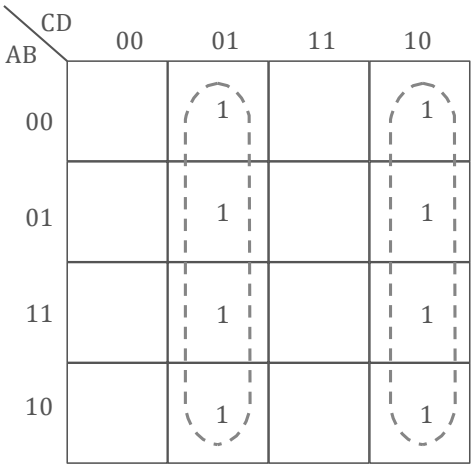
G2 · $\overline{A}$.B · $\overline{A}$.B · A · B

G3:



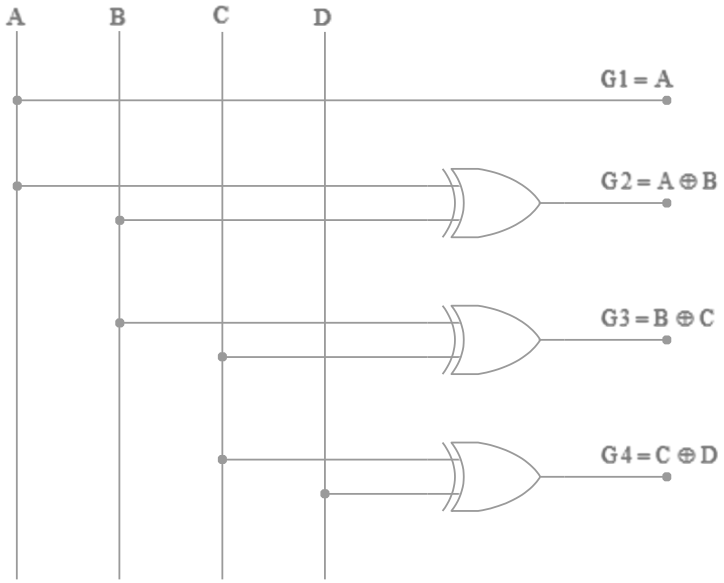
G3 · B.$\overline{C}$ · $\overline{B}$.C · B· C

G4:



$$G4 \cdot \overline{C}.D \cdot \overline{C}.D \cdot C \cdot D$$

LOGIC DIAGRAM:

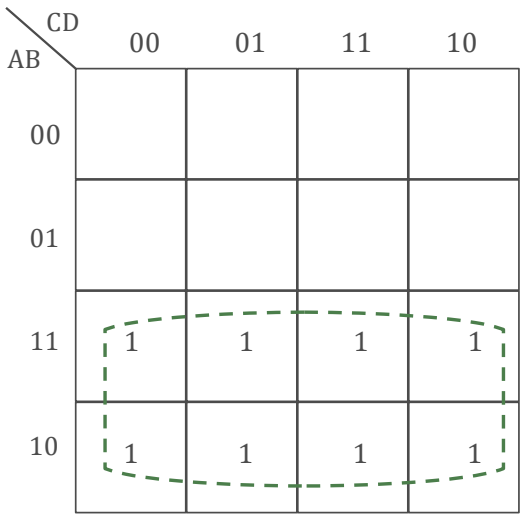


GRAY TO BINARY CODE CONVERTER:

TRUTH TABLE:

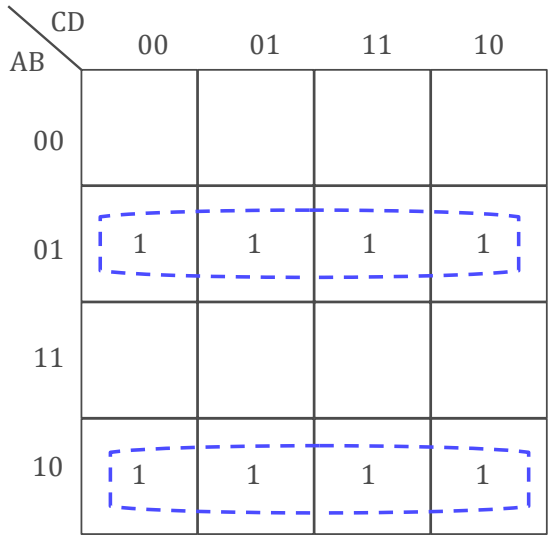
GRAY CODE				**BINARY CODE**			
A	**B**	**C**	**D**	**B1**	**B2**	**B3**	**B4**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

K-MAP:
B1:



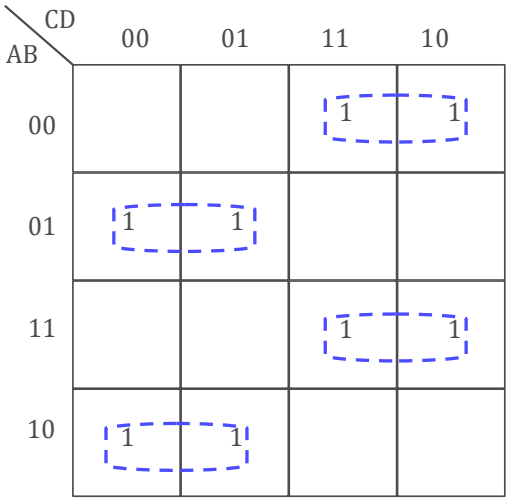
B1 = A

B2:



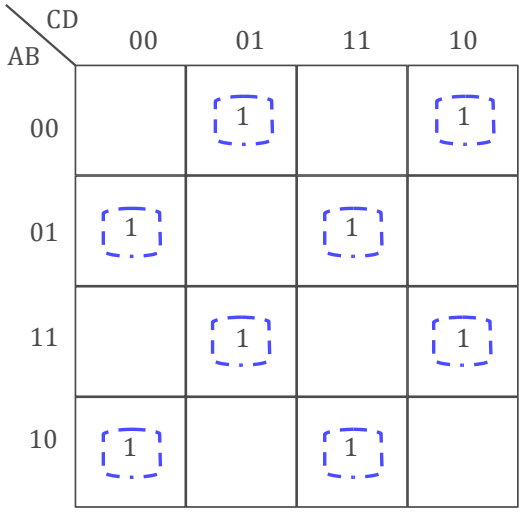
B2 = $\overline{A}B \cdot \overline{A}B \cdot A \cdot B$

B3:



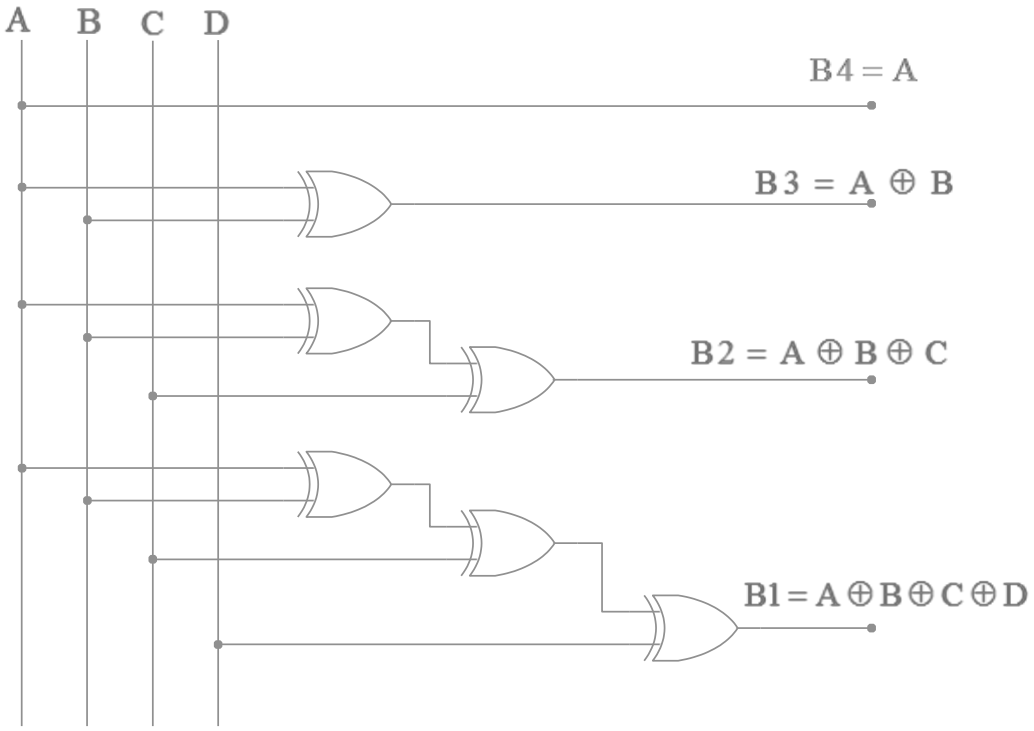
B3 = $\overline{A}\overline{B}C \cdot \overline{A}B\overline{C} \cdot A\overline{B}\overline{C} \cdot A\overline{B}C = A \cdot B \cdot C$

B4:



B4 = A · B · C · D

LOGIC DIAGRAM:



VIVA QUESTIONS:

1. What is the need for code converters?
2. Convert 1000_2 into Gray code and Excess 3 code.
3. Mention the rules for Gray to Binary code conversion.
4. Convert $(367)_{10}$ into Excess 3 code.
5. Convert the Gray coded number 10011011 to its binary equivalent.

POST-LAB QUESTIONS:

1. One use for Gray code is:

   a). coded representation of a shaft's mechanical position

   b). turning on/off software switches

   c). to represent the correct ASCII code to indicate the position of machinery

   d). to convert the angular position of machinery into hexadecimal code

2. Which of the following is not a weighted value positional numbering system:

   a). hexadecimal b). Binary-coded decimal

   c). binary d). Octal

3. Use the weighting factors to convert the following BCD numbers to binary: 0101

   0011 0010 0110 1000

   a). 01010011 001001101000 b). 11010100 100001100000

   c). 110101 100001100 d). 101011 001100001

4. In a BCD-to-seven-segment converter, why must a code converter be utilized?

   a). to convert the 4-bit BCD into 7-bit code

   b). to convert the 4-bit BCD into 10-bit code

   c). to convert the 4-bit BCD into Gray code

   d). No conversion is necessary.

5. One way to convert BCD to binary using the hardware approach is:

   a). with MSI IC circuits b). With a keyboard encoder

   c). with an ALU d). UART

RESULT:

Thus the logic diagrams are constructed and truth tables are verified for,

(a) Excess-3 to BCD

(b) BCD to Excess-3

(c) Binary to Gray code Converter

(d) Gray to Binary code converter

Ex. No. 3 Date:	PARITY GENERATOR AND PARITY CHECKER

INTRODUCTION:

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.

ANNA UNIVERSITY QUESTIONS

1. Design and construct a three bit odd and even parity generator and checker using basic gates.
   (100)
2. Design the logic circuit for the 4-bit odd parity generator and checker. (50)
3. Design the logic circuit for the 4-bit even parity generator and checker. (50)
4. Design and verify the truth table of a circuit which generates odd parity bit for three bit binary input. (50)
5. Design and verify the truth table of a circuit which generates even parity bit for three bit binary input. ` (50)

AIM:

To construct logic circuit and to verify the truth table for:

(a) Odd Parity Generator

(b) Odd Parity Checker

(c) Even Parity Generator

(d) Even Parity Checker

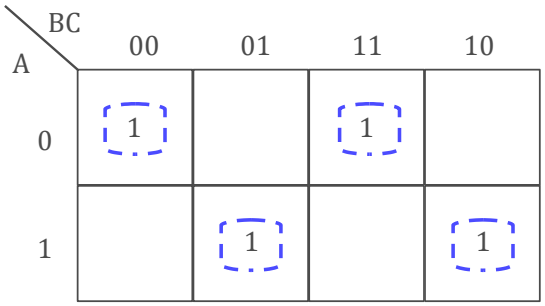
ODD PARITY GENERATOR:

TRUTH TABLE:

INPUT			OUTPUT
A	**B**	**C**	**P**
0	0	0	1

0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

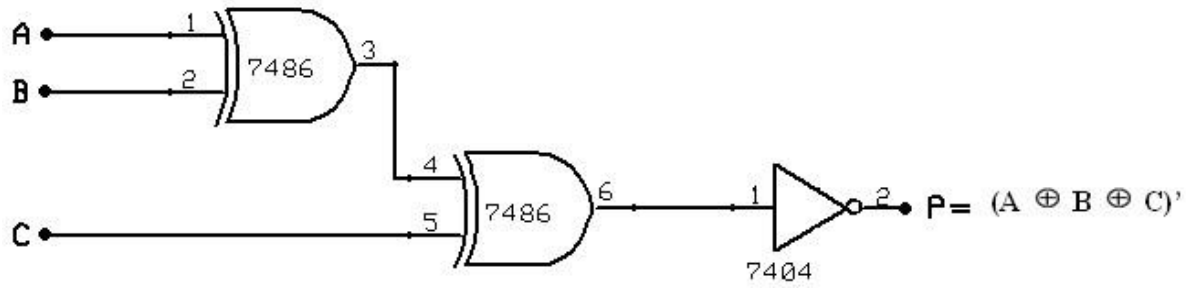
K-MAP: ODD PARITY GENERATOR:



P = · A · B· C + · A B C + A· B C + A B· C

P = $\overline{A} \cdot \overline{B} \cdot \overline{C}$

LOGIC DIAGRAM:

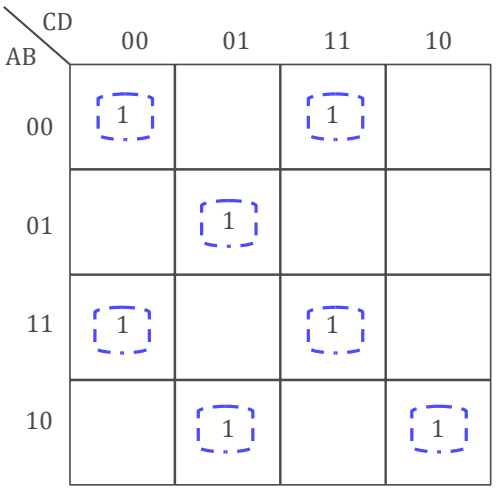


ODD PARITY CHECKER:

TRUTH TABLE:

INPUT				OUTPUT
A	**B**	**C**	**D(P)**	**P**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

K-MAP: ODD PARITY CHECKER



$$X = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{P}$$

PRE-LAB QUESTIONS

1. What is an important attribute of the conditional signal assignment statement?

   a). Its tristate outputs b). Its sequential evaluation

   c). its use of library components d). Its fast activation times

2. A simple parity-check code can detect _____ errors.

   a). an even-number of b). Two

   c). no errors d). an odd-number of

3. The Hamming distance between equal code words is _____.

   a). 1 b). n

   c). 0 d). None

4. The divisor in a cyclic code is normally called the _____.

   a). Degree b). Generator

   c). Redundancy d). None

5. In block coding, if n = 5, the maximum Hamming distance between two code words is _____.

   a). 2 b). 3

   c). 5 d). None

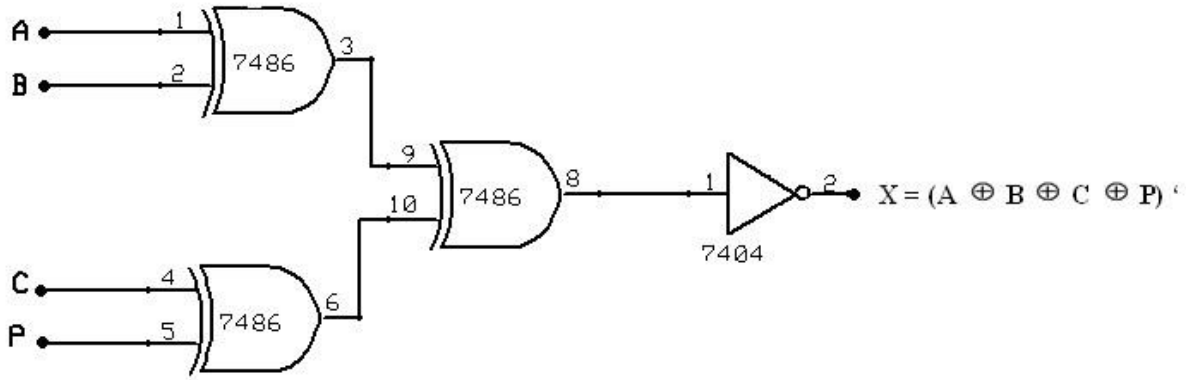
APPARATUS REQUIRED:

Sl.No	Component	Specification	Quantity
1	X-OR GATE	IC 7486	1
2	NOT GATE	IC 7404	1
3	IC TRAINER KIT	-	1
4	PATCH CORDS	-	As required

PROCEDURE:

- The logic circuit is designed using K map.
- Gates are decided for the logic circuit.
- Connections are made as per the logic diagrams.
- Apply the inputs and verify the truth table for the Parity generator and checker.

ODD PARITY CHECKER

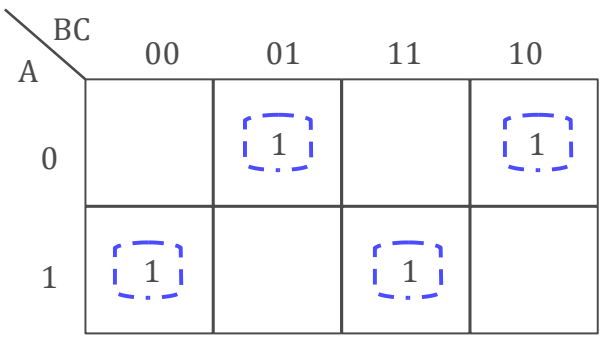


EVEN PARITY GENERATOR:

TRUTH TABLE:

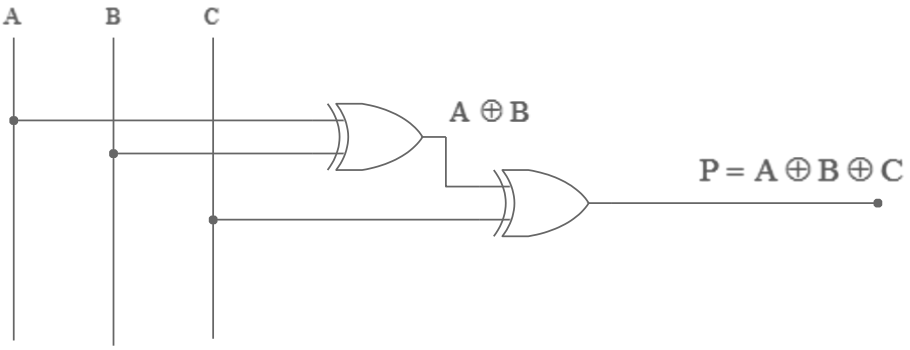
INPUT			OUTPUT
A	**B**	**C**	**P**
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

K-MAP: EVEN PARITY GENERATOR



P = A · B · C

LOGIC DIAGRAM:

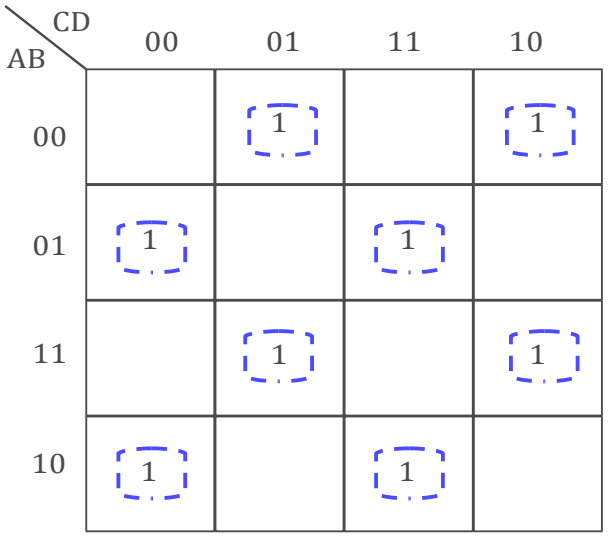


EVEN PARITY CHECKER:

TRUTH TABLE:

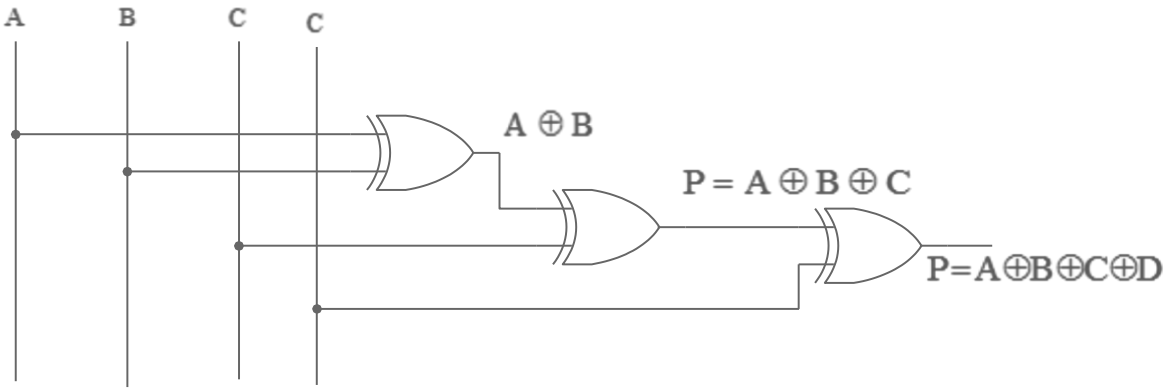
INPUT				OUTPUT
A	**B**	**C**	**D(P)**	**P**
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

K-MAP: EVEN PARITY CHECKER



P = A · B · C · D

LOGIC DIAGRAM



VIVA QUESTIONS:

1. What is parity bit?
2. What is a parity generator?
3. What is a parity checkers?
4. What is odd parity and even parity?
5. Why parity bit is added to message?

POST-LAB QUESTION:

1. While using even parity, where is the parity bit placed?

   a). Before the MSB b). After the LSB

   b). In the parity word d). After the odd parity bit

2. If odd parity is used for ASCII error detection, the number of 0s per 8-bit symbol is

   a). Even b). Odd
   c). Indeterminate d). 42

3. What VHDL techniques are used to describe a priority encoder?
   a). Integer outputs and priority coding
   b). Signal outputs and priority coding
   c). Tristate outputs and priority coding
   d). Variables and priority coding

4. Solving –11 + (–2) will yield which two's-complement answer?
   a). 1110 1101 b). 1111 1001
   c). 1111 0011 d). 1110 1001

5. The most commonly used system for representing signed binary numbers is the:
   a). 2's-complement system.
   b). 1's-complement system.
   c) 10's-complement system.
   d). sign-magnitude system.

RESULT:

Thus the logic circuits are constructed and truth tables are verified for:

(a) Odd Parity Generator

(b) Odd Parity Checker

(c) Even Parity Generator

(d) Even Parity Checker

Ex. No. 4	ENCODERS AND DECODERS
Date:	

INTRODUCTION:

ENCODER:

An encoder is digital circuit that has 2n input lines and n output lines. The output lines generate a binary code corresponding to the input values 8 - 3 encoder circuit has 8 inputs, one for each of the octal digits and three outputs that generate the corresponding binary number. Enable inputs E1 should be connected to ground and Eo should be connected to VCC.

DECODER:

A decoder is a combinational circuit that converts binary information from n input lines to 2n unique output lines. In 3-8 line decoder the three inputs are decoded into right outputs in which each output representing one of the minterm of 3 input variables.

ANNA UNIVERSITY QUESTIONS

1. Design and implement encoder using suitable IC. Verify its truth table. (100)
2. Design and implement BCD 7 segment display decoder using suitable IC. (100)
3. Design and implement 2x4 decoder using suitable logic gates and verify its truth table.
   (50)
4. Design and implement 4x2 encoder using suitable logic gates and verify its truth table.
   (50)
5. Design and construct BCD to 7 segment display decoder using dedicated decoder IC. (100)

AIM:

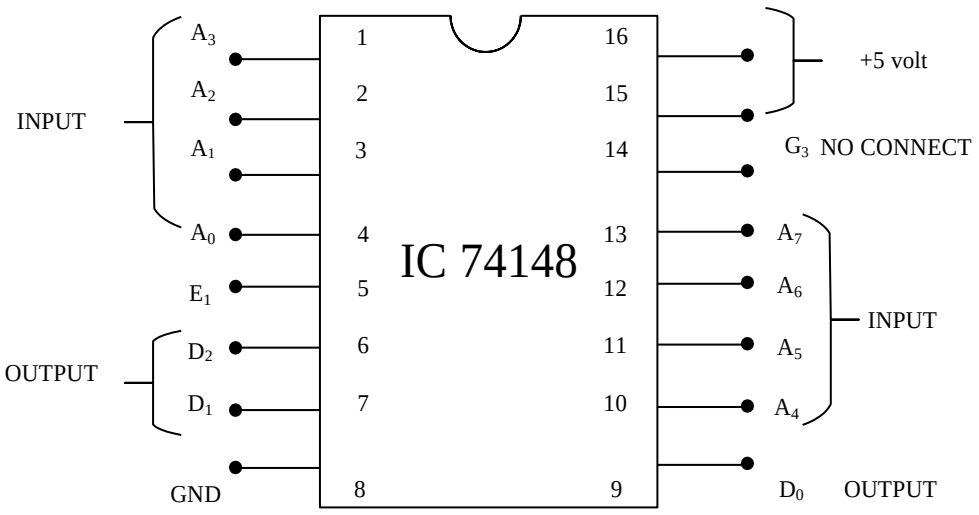
a) To design and implement encoder using IC 74148 (8-3 encoder)

b) To design and implement decoder using IC 74155 (3-8 decoder)

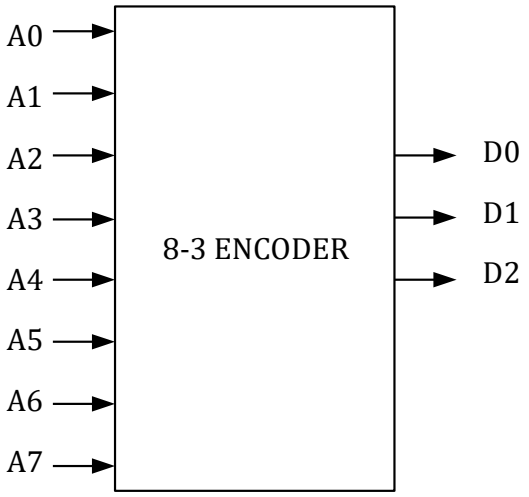
TRUTH TABLE - ENCODERS

INPUTS								OUTPUTS		
A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	D_0	D_1	D_2
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	0	1	1	1

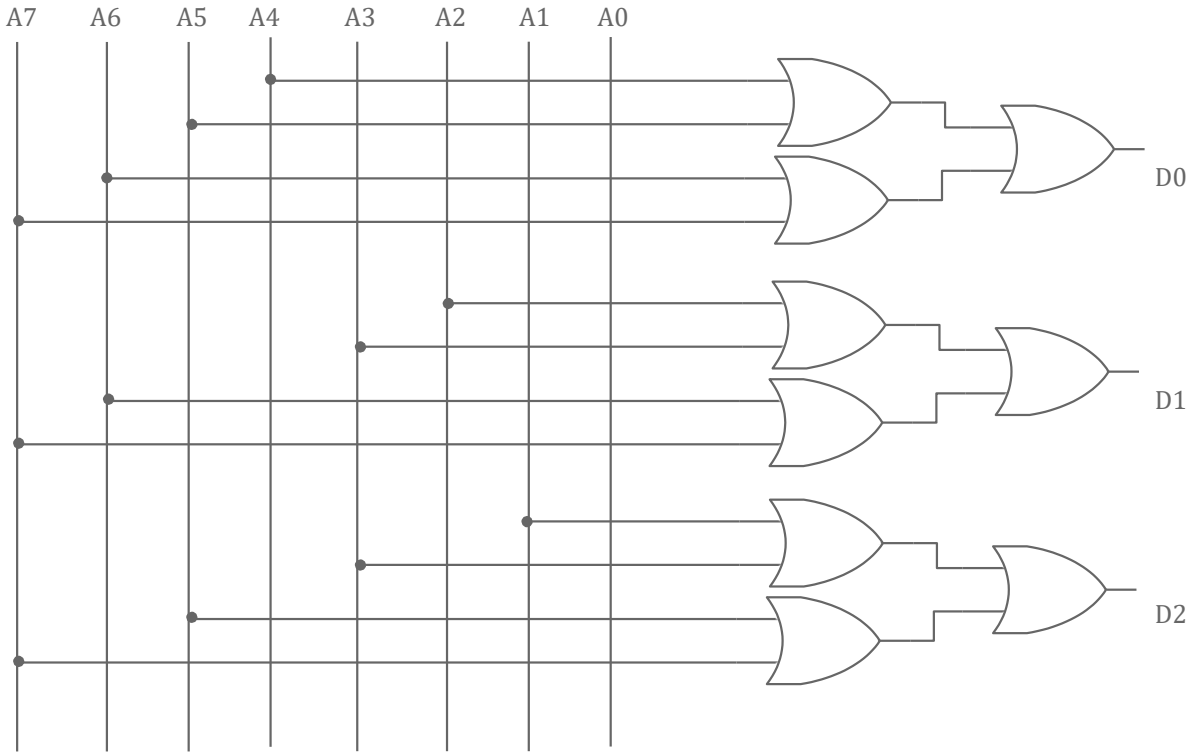
PIN DIAGRAM: ENCODER



BLOCK DIAGRAM OF 8-3 ENCODER:



CIRCUIT DIAGRAM OF 8-3 ENCODER:



PRE-LAB QUESTIONS:

1. Which digital system translates coded characters into a more useful form?
   a). Encoder b). Display
   c). Counter d). Decoder
2. A principle regarding most IC decoders is that when the correct input is present, the related output will switch:
   a). Active -high b). To a high impedance
   c). To an open d). Active -low
3. How many possible outputs would a decoder have with a 6-bit binary input?
   a). 16 b). 32
   c). 64 d). 128
4. How many inputs are required for a 1-of-16 decoder?
   a). 2 b). 4
   c). 8 d). 16
5. If two inputs are active on a priority encoder, which will be coded on the output?
   a). the higher value b). The lower value
   c). neither of the inputs d). Both of the inputs

APPARATUS REQUIRED:

S.No	Components	Specification	Quantity
1	Encoder	IC 74148	1
2	Decoder	IC 74155	1
3	OR gate	IC 7432	3
4	AND gate	IC 7408	5
5	NOT gate	IC 7404	1
6	Digital IC Trainer Kit	-	1
7	Patch chords	-	As required

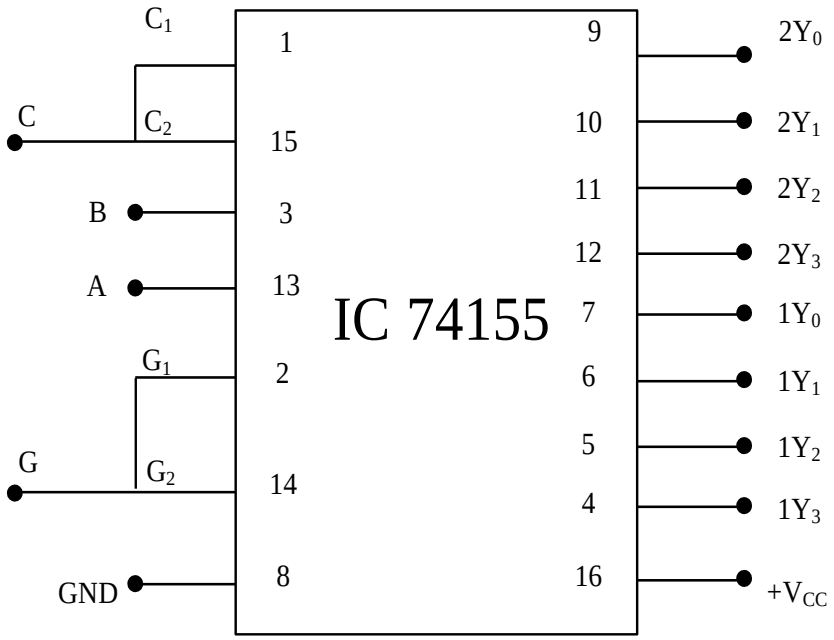
PROCEDURE:

- Connections are given as per the logic diagram.
- The truth table is verified by varying the inputs.

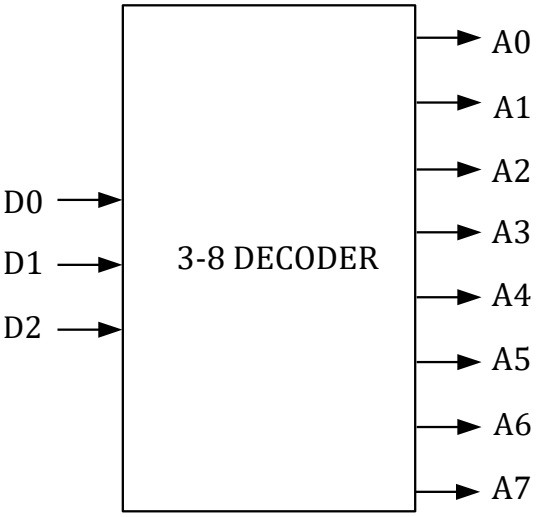
TRUTH TABLE – DECODERS:

INPUTS			OUTPUTS							
D0	**D1**	**D2**	**A7**	**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

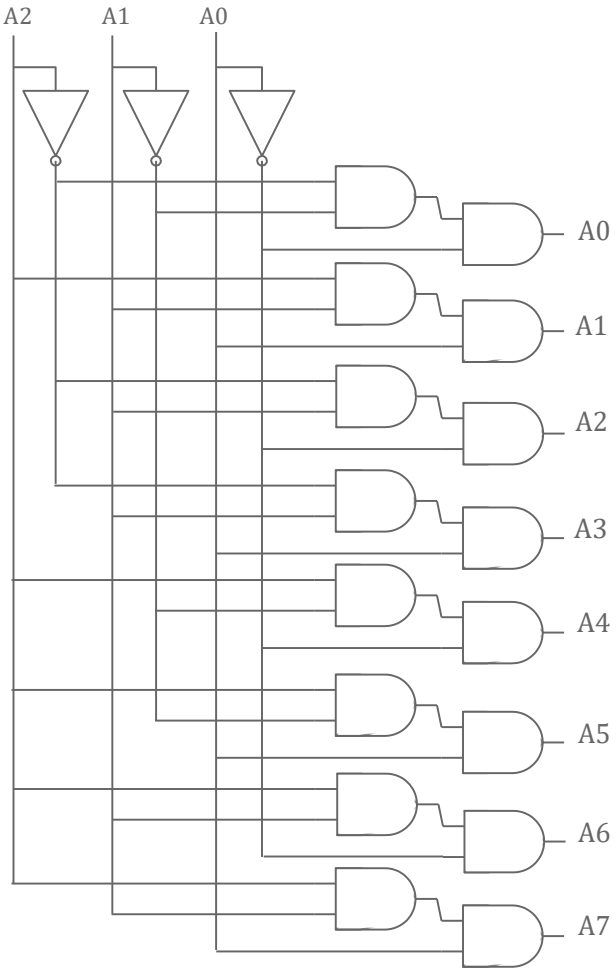
PIN DIAGRAM: DECODER



BLOCK DIAGRAM OF 3-8 DECODER



CIRCUIT DIAGRAM OF 3-8 DECODER



VIVA QUESTIONS:

1. What do you mean by encoder?
2. What is a priority encoder?
3. What are the applications of decoders?
4. Distinguish between a demultiplexer and decoder
5. List the types of decoder ICs.

POST-LAB QUESTIONS:

1. How many outputs are on a BCD decoder?

   A. 4 B. 16

   C. 8 D. 10

2. In a Gray code, each number is 3 greater than the binary representation of that number.

   A. True B. False

3. Which digital system translates coded characters into a more useful form?

   A. encoder B. Display

   C. counters D. Decoder

4. How many inputs are required for a 1-of-10 BCD decoder?

   A. 4 B. 8

   C. 10 D. 1

5. When two or more inputs are active simultaneously, the process is called:

   A. First-in, first-out processing

   B. priority encoding

   C. ripple blanking

   D. First-in, first-out processing or priority encoding

RESULT:

Thus the logic diagrams were constructed and the truth tables are verified for 8 to 3 line Encoder and 3 to 8 line Decoder.

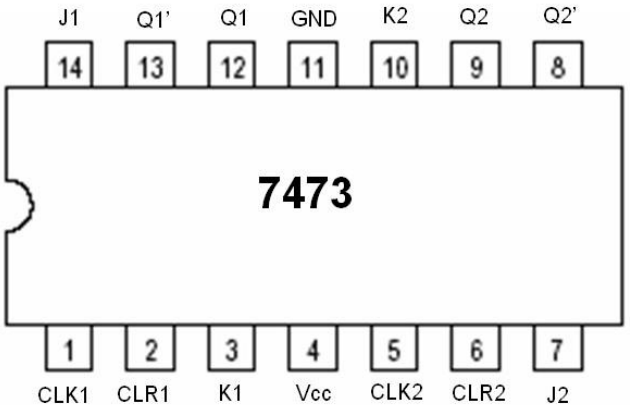
Ex. No. 5	COUNTERS
Date:	

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. An up/down counter is one that is capable of progressing in increasing order or decreasing order through a certain sequence. An up/down counter is also called bidirectional counter. Usually up/down operation of the counter is controlled by up/down signal. When this signal is high counter goes through up sequence and when up/down signal is low counter follows reverse sequence.

ANNA UNIVERSITY QUESTIONS:

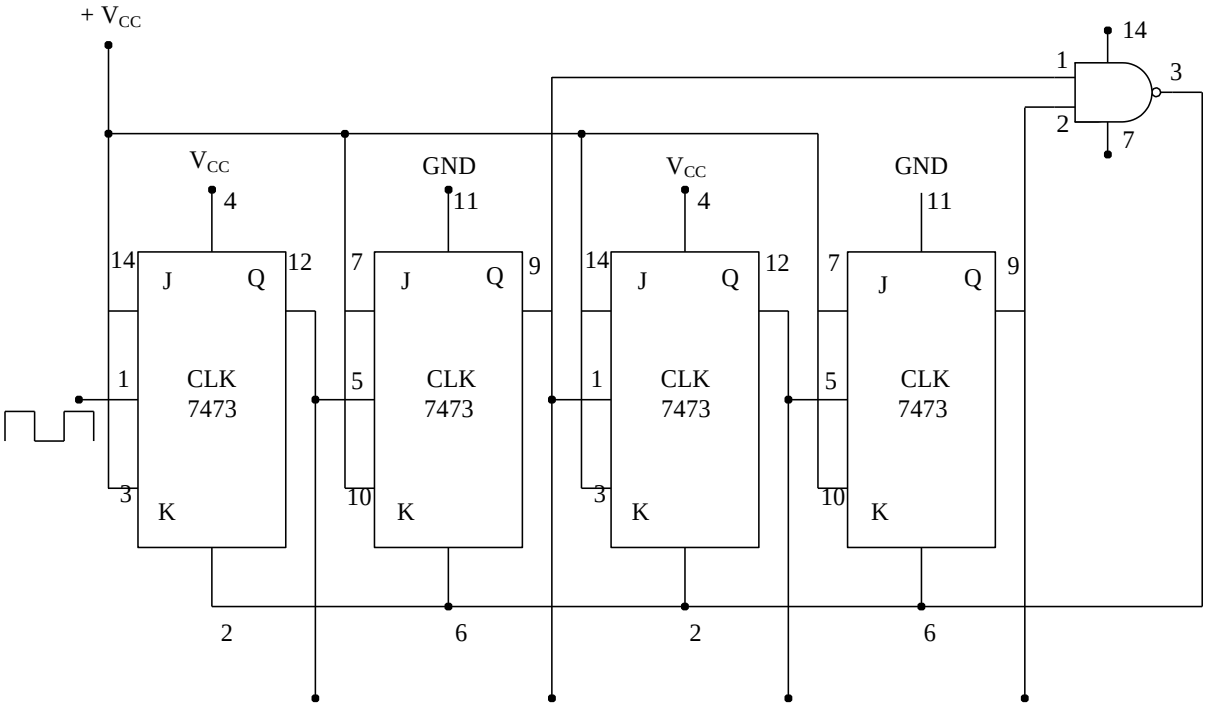
1. Design an asynchronous/ripple 4-bit binary up counter using JK flip flops.
2. Design an asynchronous/ripple 4-bit binary down counter using JK flip flops.
3. Design an asynchronous/ripple 4-bit decimal (BCD) up counter using JK flip flops.
4. Design an asynchronous/ripple 4-bit decimal (BCD down counter using JK flip flops.
5. Design a 4 bit synchronous binary up counter using JK flip flops.

PIN DIAGRAM OF IC 7473:



:

CIRCUIT DIAGRAM (ASYNCHRONOUS COUNTER):



TRUTH TABLE:

Clock Count	Output				Decimal Value
	Q_D	Q_C	Q_B	Q_A	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its output back to zero				

AIM:

To implement and verify the truth table of synchronous and asynchronous counter.

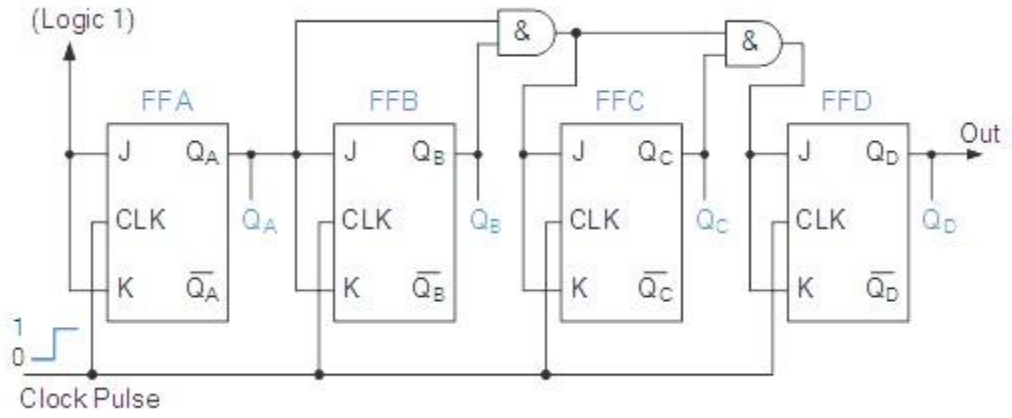
APPARATUS REQUIRED:

S. No	Components	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7473	2
4.	NAND gate	IC 7400	1
5.	AND gate	IC 7408	1
6.	Connecting wires		As required

PROCEDURE:

- Connections are given as per the logic diagram.
- The truth table is verified by varying the inputs.

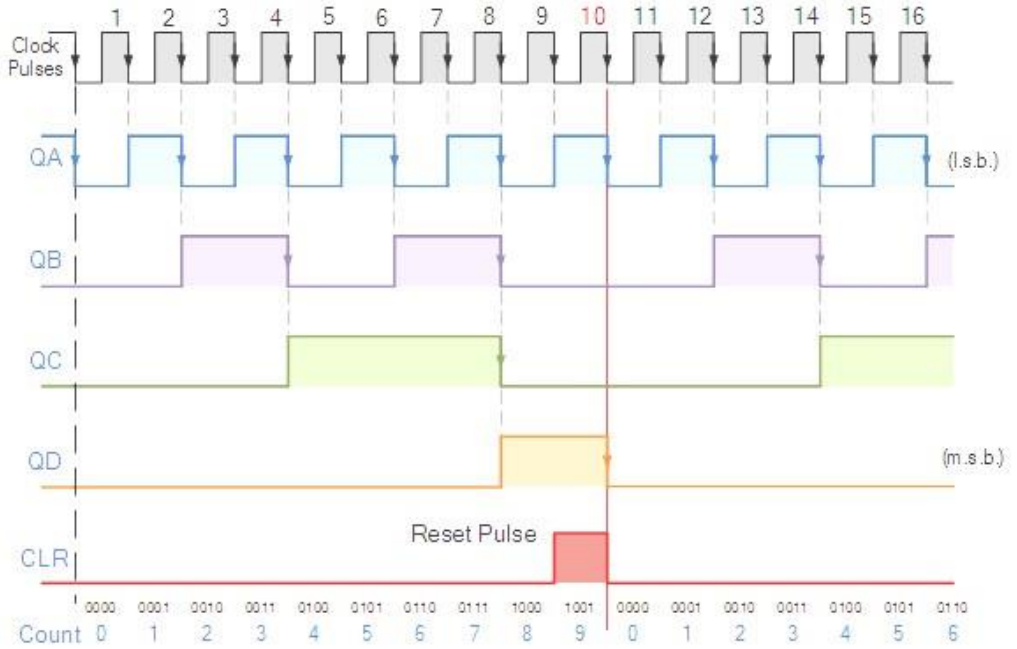
CIRCUIT DIAGRAM (ASYNCHRONOUS COUNTER):



TRUTH TABLE:

Clock Count	Output				Decimal Value
	Q_D	Q_C	Q_B	Q_A	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	1	0	1	0	10
12	1	0	1	1	11
13	1	1	0	0	12
14	1	1	0	1	13
15	1	1	1	0	14
16	1	1	1	1	15
17	Counter Resets its output back to zero				

Decade Counter Timing Diagram



VIVA QUESTIONS:

1. Define clock.
2. Define clock period.
3. What is flip-flop?
4. Define counter.
5. What is an asynchronous counter?

PRE-LAB QUESTIONS:

1. The terminal count of a modulus-11 binary counter is _____.

   a). 1010 b). 1000

   c). 1001 d). 1100

2. Synchronous construction reduces the delay time of a counter to the delay of:

   a). All flip-flops & gates b). All flip-flops and gates a 3 count

   c). A single gate d). A single flip-flop & a gate

3. A BCD counter is a _____.

   a). binary counter b). Full-modulus counter

   c). decade counter d). divide-by-10 counter

4. How many different states does a 3-bit asynchronous counter have?

   a). 2 b). 4

   c). 8 d). 16

5. The final output of a modulus-8 counter occurs one time for every _____.

   a). 8 clock pulses b). 16 clock pulses

   c). 24 clock pulses d). 32 clock pulses

POST-LAB QUESTION:

1. If both inputs of a gated S-R flip-flop are LOW, what will happen when the flip-flop is enabled?

   a). No change will occur in the output b). An invalid state will exist

   c). The output will toggle. d). The output will reset.

2. The parallel outputs of a counter circuit represent the:

   a). parallel data word b). clock frequency

   c). counter modulus d). clock count

3. The One example of the use of an S-R flip-flop is as a(n):

   a). racer

   b). astable oscillator

   c). binary storage register

d). transition pulse generator

4. One of the major drawbacks to the use of asynchronous counters is:

   a). low-frequency applications are limited because of internal propagation delays

   b). high-frequency applications are limited because of internal propagation delays

   c). asynchronous counters do not have major drawbacks and are suitable for use in high- and low-frequency counting applications

   d). asynchronous counters do not have propagation delays and this limits their use in high-frequency applications

5. Synchronous counters eliminate the delay problems encountered with asynchronous counters because the:

   a). input clock pulses are applied only to the first and last stages

   b). input clock pulses are applied only to the last stage

   c). input clock pulses are not used to activate any of the counter stages

   d). input clock pulses are applied simultaneously to each stage

RESULT:

The truth table of Asynchronous counter and Synchronous counter was verified.

Ex. No. 6 Date:	SHIFT REGISTERS

The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name "shift register". A register capable of shifting its binary information either to the left or to the right is called a shift register. The logical configuration of a shift register consists of a chain of flip flops connected in cascade with the output of one flip flop connected to the input of the next flip flop. All the flip flops receive a common clock pulse which causes the shift from one stage to the next.

ANNA UNIVERSITY QUESTIONS

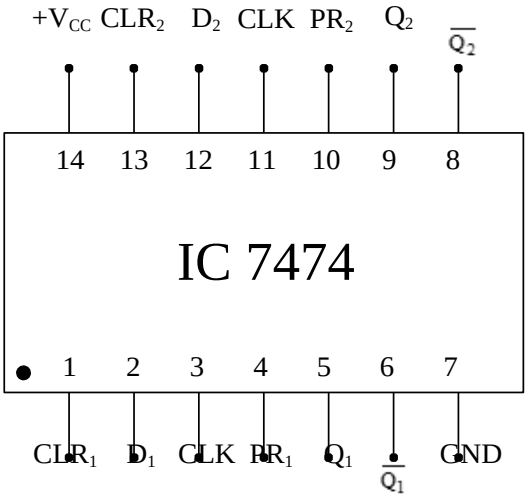
1. Design and construct a 4-bit shift register in SISO, SIPO, PISO and PIPO modes using suitable ICs. (100)
2. Design & construct a 4 bit Serial in serial out shift register. (100)
3. Design & construct a 4 bit Serial in parallel out shift register. (100)
4. Design & construct a 4 bit Parallel in serial out shift register. (100)
5. Design & construct a 4 bit Parallel in parallel out shift register. (100)

AIM:

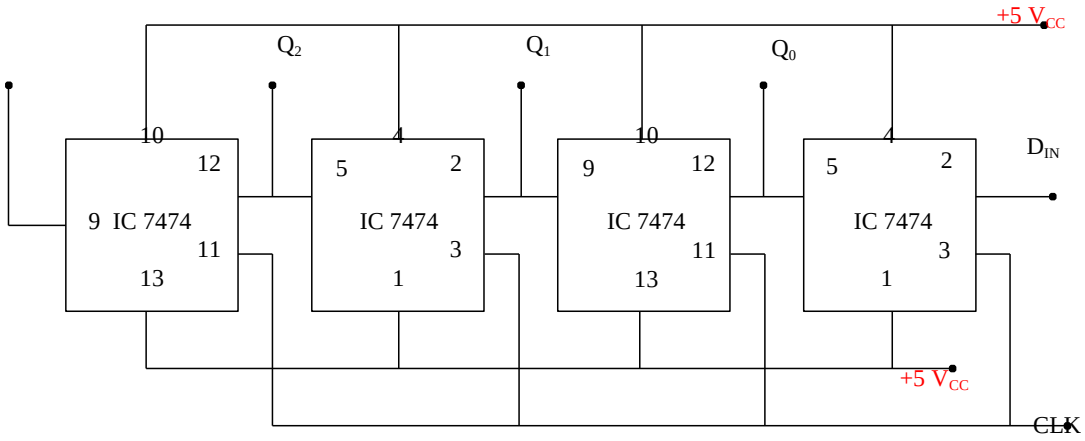
To implement the following shift register using flip flop

(i) SIPO (ii) SISO (iii) PISO (iv) PIPO

PIN DIAGRAM IC7474:



SIPO- LEFT SHIFT:



APPARATUS REQUIRED:

S. No	Component	Specification	Quantity
1.	IC	7474	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

PROCEDURE:

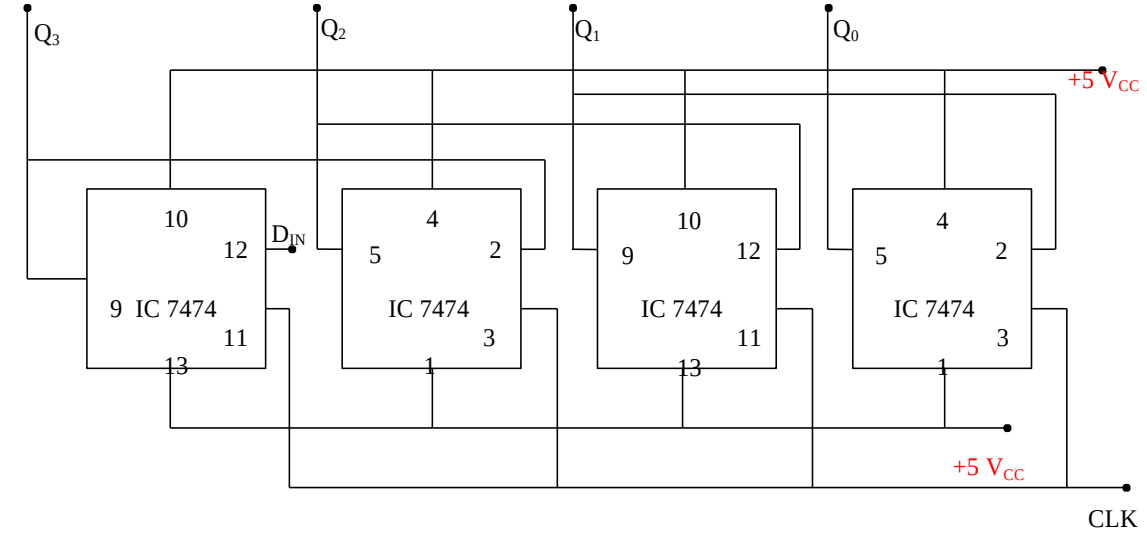
- Give the connections as per the circuit.
- Set or Reset at pin no:2 which is the MSB of serial data
- Apply a single clock Set or Reset second digital input at pin no:2.
- Repeat step 2 until all 4-bit data are taken away.

VERIFICATION TABLE:

No of clock pulse	Serial input D_{in}	Parallel output			
		Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1

3	0	0	1	1	0
4	1	1	1	0	1
5	0	1	0	1	0
6	0	0	1	0	0
7	0	1	0	0	0
8	0	0	0	0	0

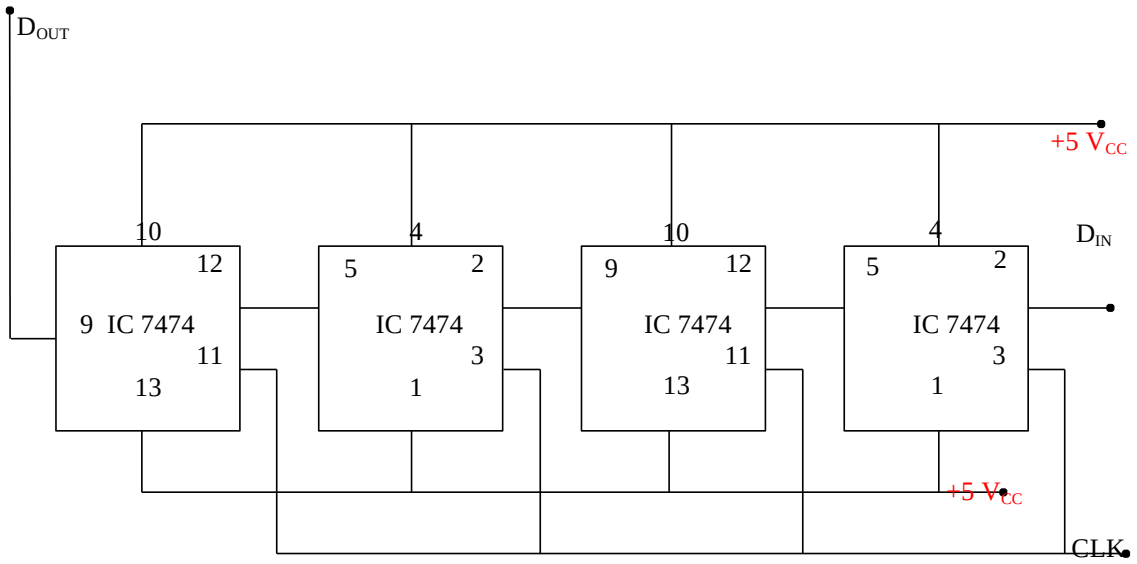
SIPO- RIGHT SHIFT:



VERIFICATION TABLE:

No of clock pulse	Serial input D_{in}	Parallel output			
		Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0
1	1	1	0	0	0
2	1	0	1	0	0
3	0	1	0	1	0
4	1	1	1	0	1
5	0	0	1	1	0
6	0	0	0	1	1
7	0	0	0	0	1
8	0	0	0	0	0

SISO:

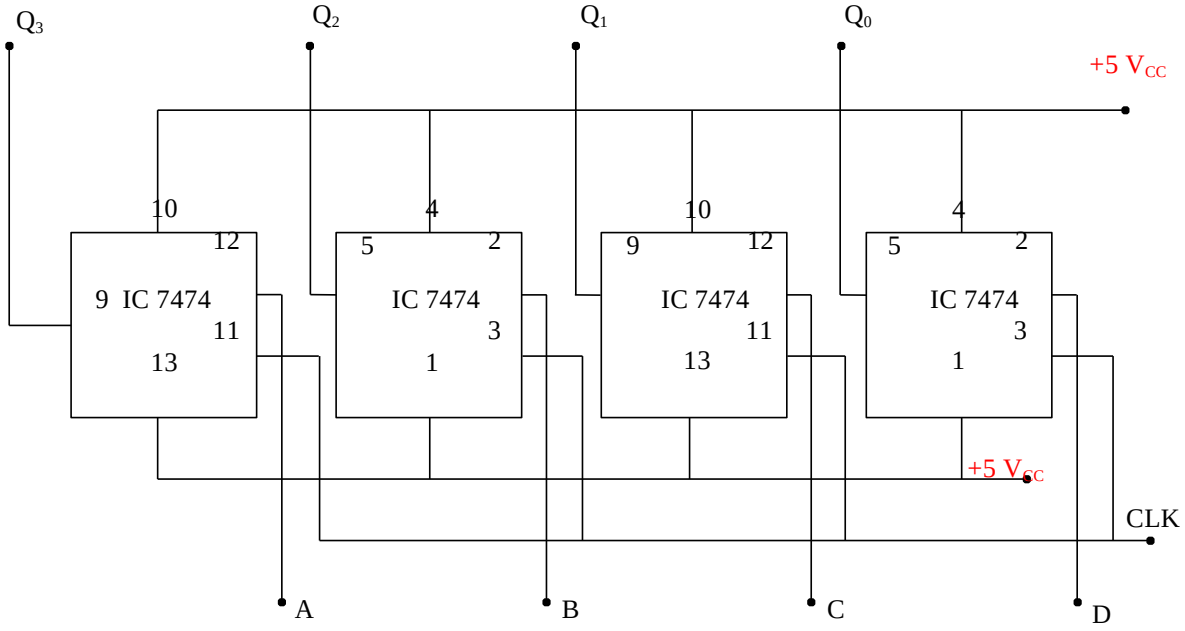


VERIFICATION TABLE:

Data input = 1100

Clock	Serial input	Serial output
0	0	0
4	1	1
8	1	1
12	0	0
16	0	0

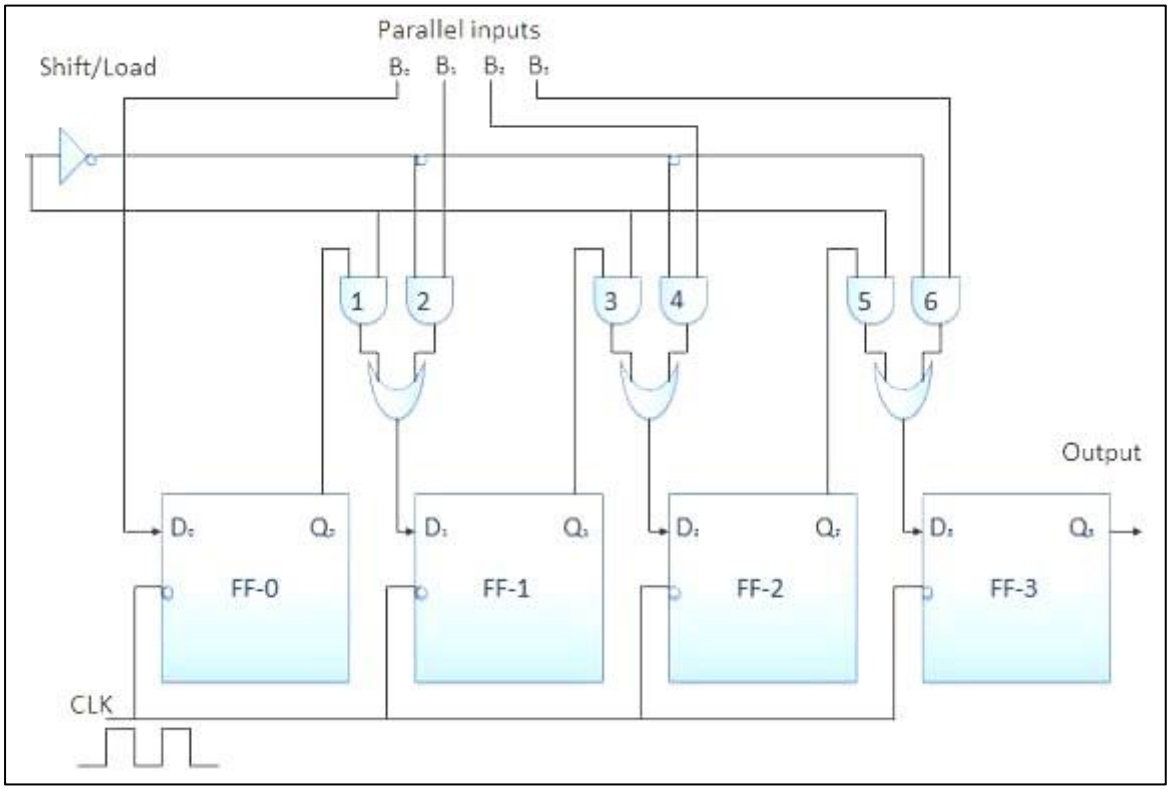
PIPO:



VERIFICATION TABLE:

Clock	Parallel input				Parallel output			
	A	**B**	**C**	**D**	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1

PISO:



PRE-LAB QUESTIONS:

1. How is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?

   a). Tristate b). End around

   c). Universal d). Conversion

2. How much storage capacity does each stage in a shift register represent?

   a). One bit b). Two bits

   c). Four bits d). Eight bits

3. Which is not the characteristic of a shift register?

   a). Serial in/parallel in b). Serial in/parallel out

   c). Parallel in/serial out d). Parallel in/parallel out

4. A 74HC195 4-bit parallel access shift register can be used for _____.

   a). serial in/serial out operation b). Serial in/parallel out operation

   c). parallel in/serial out operation d). All of the above

5. How many clock pulses will be required to completely load serially a 5-bit shift register?

   a). 2 b). 3

   c). 4 d). 5

VIVA QUESTIONS:

1. Define shift register.
2. What are the different types of shift registers?
3. Mention the applications of shift registers.
4. What is a register?
5. What is shift register counter?

POST-LAB QUESTIONS:

1. Another way to connect devices to a shared data bus is to use a _____.

   a). circulating gate b). Transceiver

   c). bidirectional encoder d). strobed latch

2. A 4-bit shift register that receives 4 bits of parallel data will shift to the by

   _____ position(s) for each clock pulse.

   a). right, one b). right, two

   c). left, one d). left, three

3. Computers operate on data internally in a _____ format.

   a). tristate b). universal

   c). parallel d). serial

4. By adding recirculating lines to a 4-bit parallel-in, serial-out shift register, it becomes a _____, _____, and _____-out register.

   a). parallel-in, serial, parallel b). serial-in, parallel, serial

   c). series-parallel-in, series, parallel d). bidirectional in, parallel, series

5. One purpose of a three-state buffer is:

   a). to provide isolation between the input device and the data bus

   b). to provide the sink or source current required by any device connected to its output without loading down the output device

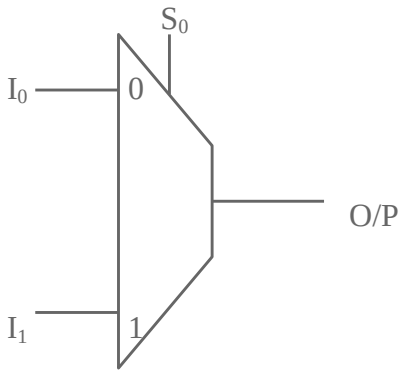
   c). temporary data storage

   d). to control data flow

RESULT:

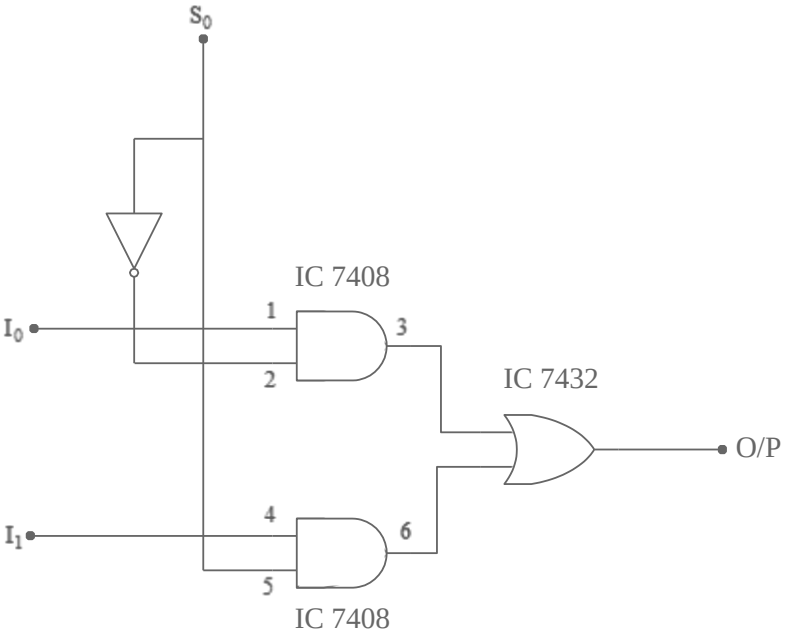
Thus the SISO, SIPO, PISO, PIPO shift registers were designed and implemented.

a) 2: 1 MULTIPLEXER:

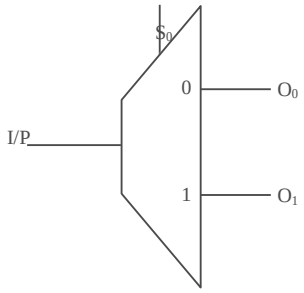


S_0	O/P
0	I_0
1	I_1

LOGIC DIAGRAM:



b) 1: 2 DE MULTIPLEXER:



S_0	I/P at
0	O_0
1	O_1

Ex. No. 7 Date:	MULTIPLEXER AND DEMULTIPLEXER

INTRODUCTION:

Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

ANNA UNIVERSITY QUESTIONS:

1. Design & implement 1x4 demultiplexer by using suitable logic gates & verify its truth table (100)
2. Design & implement 4x1 Multiplexer by using suitable logic gates & verify its truth table (100)
3. Design 1:4 de multiplexer using suitable ICs. (100)
4. Design 4:1 multiplexer using suitable ICs. (100)

AIM:

To construct the logic diagram and verify the truth table for:

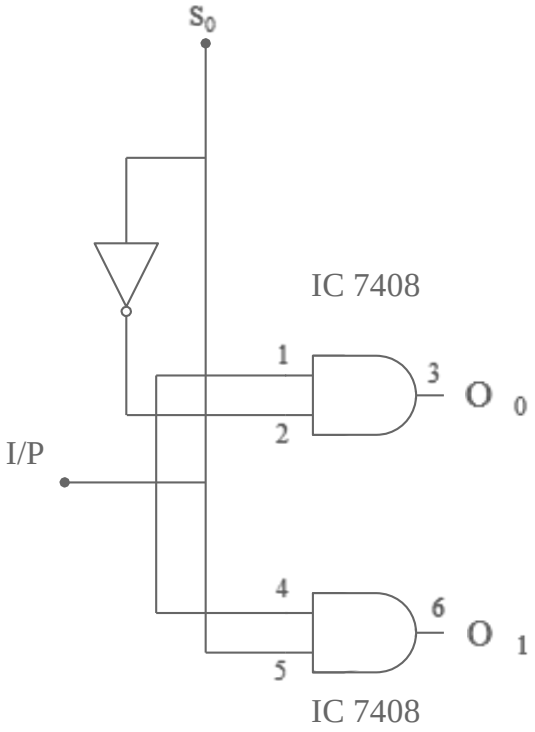
(a) 2:1 Multiplexer

(b) 1: 2 De multiplexer

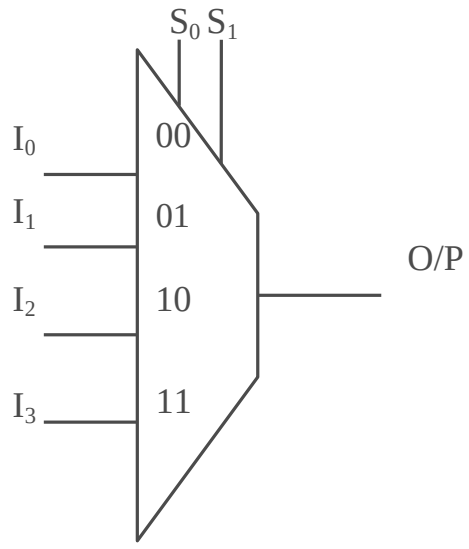
(c) 4:1 Multiplexer.

(d) 1: 4 De multiplexer.

LOGIC DIAGRAM:



a) 4: 1 MULTIPLEXER:



S_0	S_1	O/P
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

PRE-LAB QUESTIONS:

1. What is the function of an enable input on a multiplexer chip?
   a). To apply Vcc b). To connect ground
   c). To active the entire chip d). To active one half of the chip
2. A basic multiplexer principle can be demonstrated through the use of a:
   a). Single pole relay b). DPDT switch
   c). Rotary switch d). Linear stepper
3. Most de multiplexers facilitate which type of conversion?
   a). Decimal-Hex b). Single input, multiple outputs
   c). AC-DC d). Odd parity to Even parity
4. The inputs/outputs of an analog multiplexer/demultiplexer are:
   a). bidirectional b). Unidirectional
   c). even parity d). Binary-coded decimal
5. One application of a digital multiplexer is to facilitate:
   a). data generation b). Serial-to-parallel conversion
   c). parity checking d). Data selector

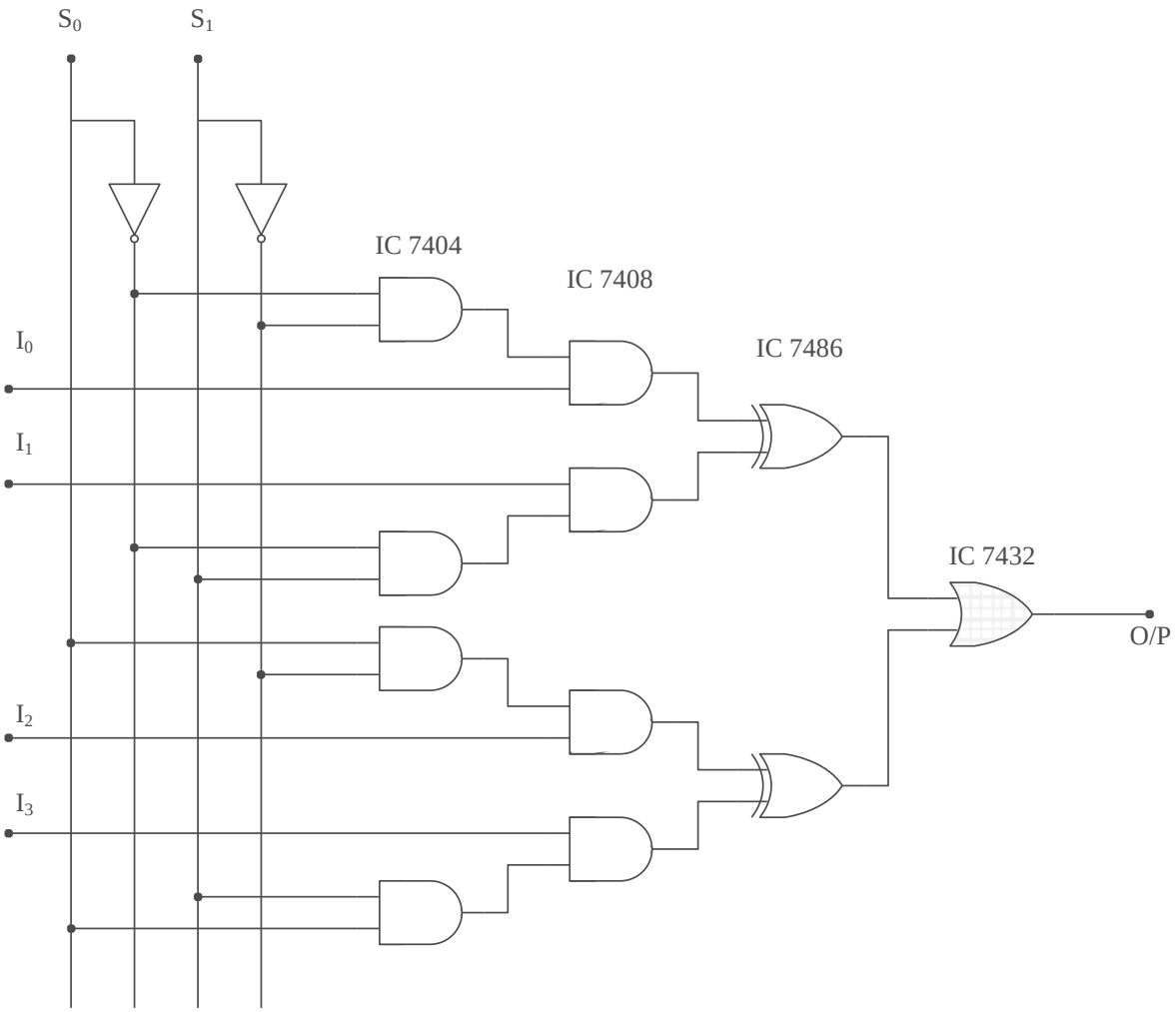
APPARATUS REQUIRED:

Sl.No	Component	Specification	Quantity
1	X-OR Gate	IC 7486	1
2	NOT Gate	IC 7404	1
3	AND Gate	IC 7408	1
4	OR Gate	IC 7432	1
5	IC TRAINER KIT	-	1
6	PATCH CORDS	-	As required

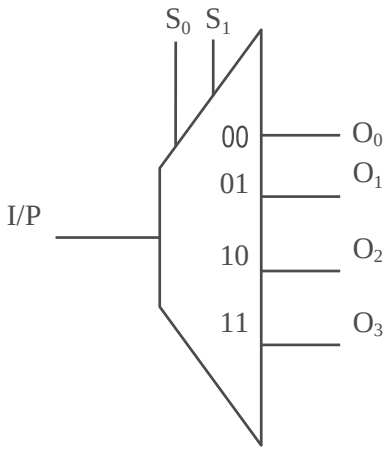
PROCEDURE:

1. Connections are made as per the logic diagram.
2. The truth tables are verified.

LOGIC DIAGRAM:

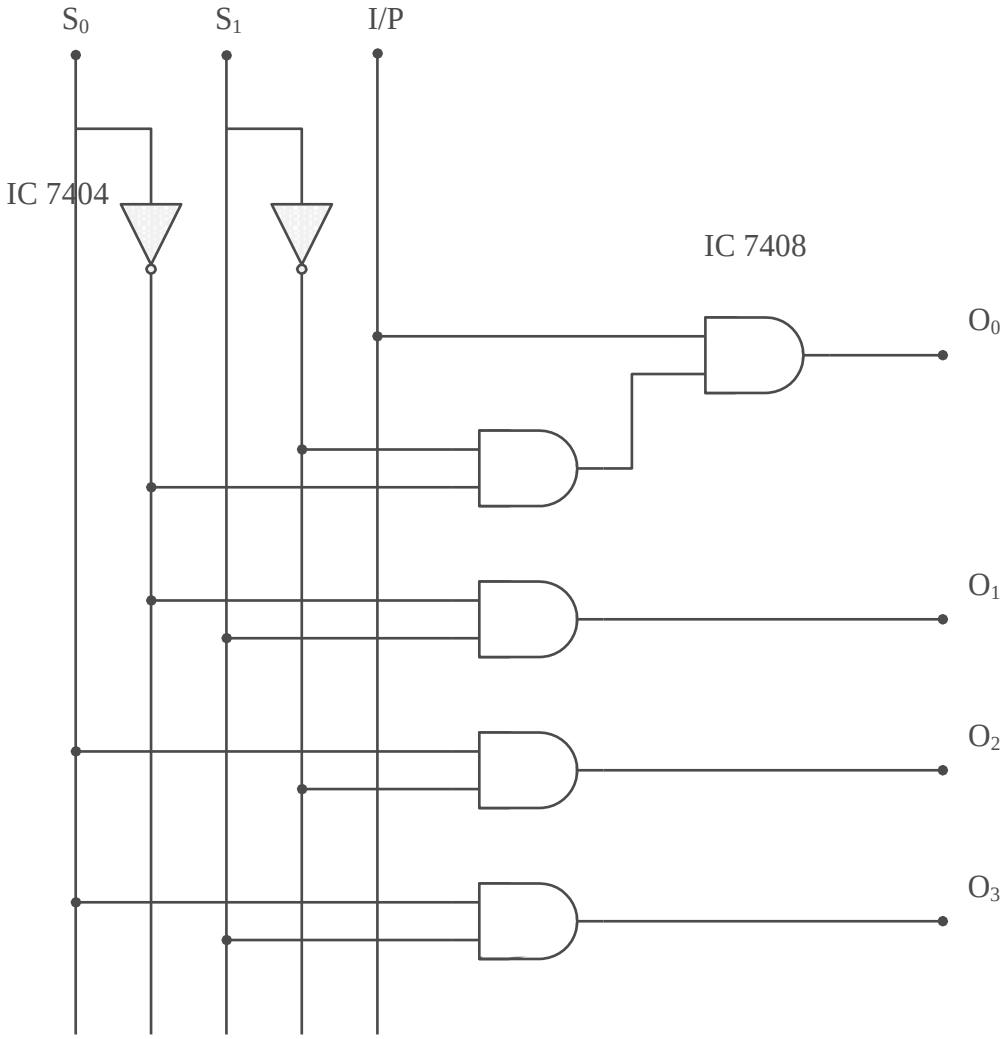


b) 1: 4 DE MULTIPLEXER:



I/P	**S_0**	**S_1**	**O_0**	**O_1**	**O_2**	**O_3**
1	X	0	0	0	0	0
0	0	0	0	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

LOGIC DIAGRAM:



VIVA QUESTIONS:

1. What is a data Multiplexer?
2. Give an application for a multiplexer.
3. Give an application for a de multiplexer.
4. List some of the commonly used multiplexer ICs.
5. What is Demultiplexer?

POST-LAB QUESTIONS:

1. One application of a digital multiplexer is to facilitate:
   a). data generation b). Serial-to-parallel conversion
   c). parity checking d). Data selection
2. One multiplexer can take the place of:
   a). several SSI logic gates b). Combinational logic circuits
   c). several Ex-NOR gates
   d). several SSI logic gates or combinational logic circuits
3. The inputs/outputs of an analog multiplexer/demultiplexer are:
   a). bidirectional b). Unidirectional
   c). even parity d). Binary-coded decimal
4. A basic multiplexer principle can be demonstrated through the use of a:
   a). single-pole relay b). DPDT switch
   c). rotary switch d). Linear stepper
5. One can safely state that the output lines for a demultiplexer are under the direct control of the:
   a) input data select lines b) the internal AND gates
   c) the internal OR gate. d) Input data line.

RESULT:

Thus logic diagrams are constructed and truth tables are verified for

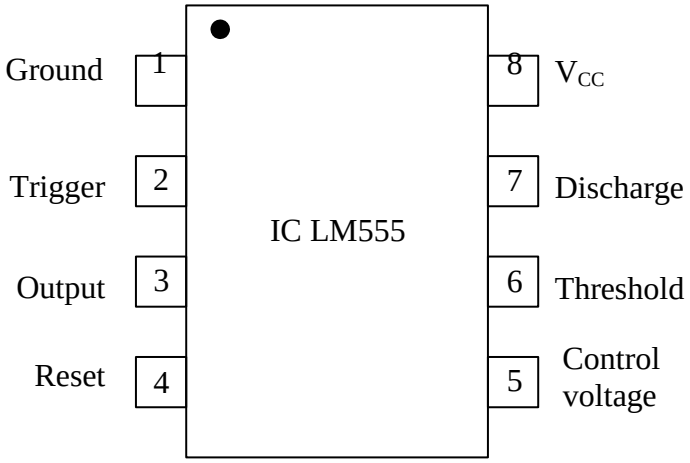
(a) 2:1 Multiplexer

(b) 1: 2 De multiplexer

(c) 4:1 Multiplexer.

(d) 1: 4 De multiplexer.

PIN DIAGRAM:


Ground
1
Trigger
2
Output
3
Reset
4
IC LM555
8
V_{CC}
7
Discharge
6
Threshold
5
Control voltage

Ex. No. 8	TIMER IC (555) APPLICATION
Date:	

INTRODUCTION:

ASTABLE MULTIVIBRATOR:

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. This circuit does not require an external trigger to change the state of the output. The time during which the output is either high or low is determined by two resistors and a capacitor, which are connected externally to the 555 timer. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by,

$$t_c = 0.69 (R_1 + R_2) C$$

Similarly the time during which the capacitor discharges from 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by,

$$t_d = 0.69 (R_2) C$$

Thus the total time period of the output waveform is,

$$T = t_c + t_d = 0.69 (R_1 + 2 R_2) C$$

$$\% \text{ duty cycle} = [(R_1 + R_2) / (R_1 + 2 R_2)] \times 100$$

MONOSTABLE MULTIVIBRATOR:

A monostable multivibrator often called a one-shot multivibrator is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand-by state the output of the circuit is approximately zero or at logic low level. When an external trigger pulse is applied, the output is forced to go high (approx. V_{cc}). The time during which the output remains high is given by,

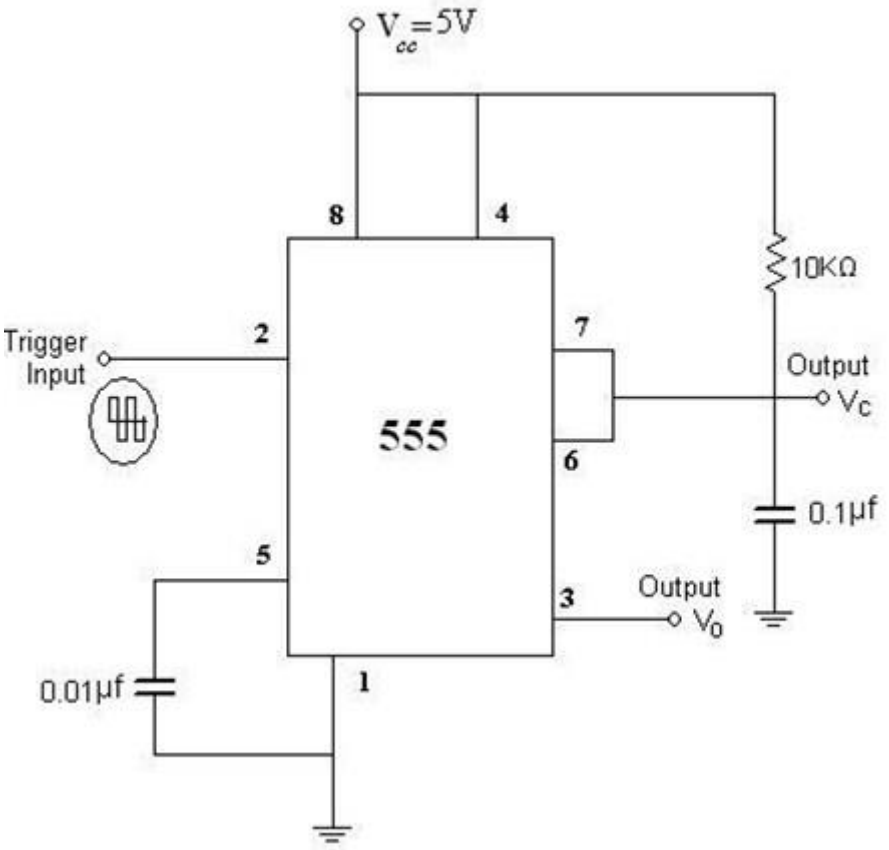
$$t_p = 1.1 R_1 C$$

ANNA UNIVERSITY QUESTIONS:

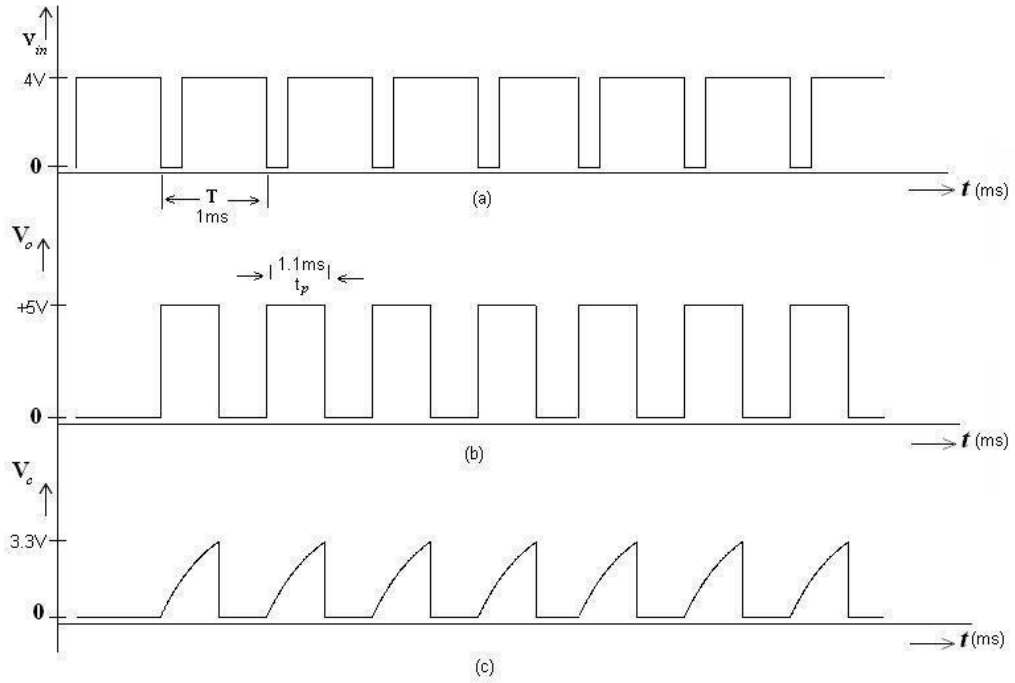
1. Construct an astable multivibrator using IC555 timer & to generate a 1KHz square waveform. (100)
2. Construct a circuit Operate the IC555 timer in Monostable mode to generate a 1KHz square waveform. (100)
3. Design and construct an astable multivibrator using IC 555 for square wave generation. (100)
4. Design and construct a monostable multivibrator using IC 555 for pulse wave generation. (100)
5. Design a free running multivibrator using 555 timer to obtain an output waveform of frequency 1 KHz and duty cycle of 75%. (100)

a) MONOSTABLE MULTIVIBRATOR:

CIRCUIT DIAGRAM:



Model Graph:



AIM:

(a) To design and obtain the Mono stable multivibrator using IC555 timer for the given time period.

(b) To design and obtain the Astable multivibrator using IC555 timer for the given time period.

To design and test an astable multivibrator for generating symmetrical and unsymmetricalsquare wave form for the given frequency and duty cycle.

APPARATUS REQUIRED:

S. No.	Name of the Apparatus	Range/Value	Qty
1.	Bread Board	-	1
2.	Resistor	3.6 k Ω, 7.2 k Ω	1, 2
3.	IC 555	-	1
4.	CRO	20 MHz.	1
5.	Capacitor	0.1µF, 0.01µF	1, 1
6.	RPS	(0-30) V/ 5V	1
7.	Diode		1
8.	Connecting Wires	-	Few

THEORY:

The 555 timer is connected as an astable multivibrator as shown in figure. In this mode of operation the timing capacitor charges up towards V_{cc} (assuming V_o is high initially) through ($R_a + R_b$) until the voltage across the capacitor reaches the threshold level (2/3) V_{cc}. At this point the internal upper comparator switches state causing the internal flip-flop output to go high. This turns on the discharge transistor and the timing capacitor C then discharges through R_b and the discharging
transistor. The discharging continues until the capacitor voltage drops to (1/3) V_{cc} at which point the internal lower comparator switches states causing the internal flip-flop output to go low, turning off the discharge transistor. At this point the capacitor starts to charge again, thus completing the cycle.

DESIGN:

i. For Unsymmetrical waveform:

$f = 1/T = 1.44/(R_a+2R_b)C$;

$DutyCycle = D = t_{low}/ (t_{low} + t_{high}) =>$

$D = R_b/ (R_a +2R_b)$;

Where $t_{high} = 0.693(R_a + R_b)C$; $t_{low} = 0.69$;

Specifications: frequency = 1kHz;

Duty cycle = 25%Design:

$t_{low} = 0.25ms = 0.693R_b C$;

Let $C = 0.1\mu F => R_b = 0.25/(0.693X0.1X10^{-6}) =$

$t_{high} = 0.693(R_a + R_b)C = 0.75$ ms => $R_a =$

ii. For Symmetrical Wave form :

$t_{high} = 0.693 R_a C$; $t_{low} = 0.693 R_b C$

$f = 1/T = 1.44 /(R_a + R_b)C => D = R_b /(R_a + R_b)$;

Specifications: frequency = 1 kHz; Duty cycle = 50% .Design: t_{low} = 0.5 ms = 0.693 R_bC;

Let C= 0.1 µF; R_b =

t_{high} = 0.693 R_a C = 0.5 ms ; R_a =

PRE-LAB QUESTIONS:

1. Which of the following is not a characteristic of a retriggerable monostable multivibrator?

   a). Dual multivibrator b). Active high reset

   c). It has no internal resistor d). None

2. Pulse stretching, time-delay, and pulse generation are all easily accomplished with which type of multivibrator circuit?

   a). Astable b). Monostable

   c). Multistable d). Bistable

3. What is the other name for a bistable multivibrator?

   a). On-off switch b). Oscillator

   c). Flip-flop d). None

4. An astable multivibrator requires:

   a). Balanced time constants b). A pair of matched transistors

   c). No input signal d). Dual J-K flip flops

5. What controls the output pulse width of a one-shot?

   a). The clock frequency b). The width of the clock pulse

   c). An RL time constant d). An RC time constant

APPARATUS REQUIRED:

S.No.	Components	Range	Quantity
1	IC LM555 Timer		1
2	Resistor	10KΩ	1
3	Capacitor	0.01µF,	1
4	Capacitor	0.1µF	1
5	RPS	(0- 30)V	1
6	CRO		1
7	Function Generator		1
8	Bread Board		1
9	Connecting Wires		

DESIGN:

Consider VCC = 5V, for given tp Output pulse width tp = 1.1 R_A C

Assume C in the order of microfarads & Find R_A

Typical values:

If C=0.1 μF , RA = 10k then tp = 1.1 m Sec ,Trigger Voltage =4 V

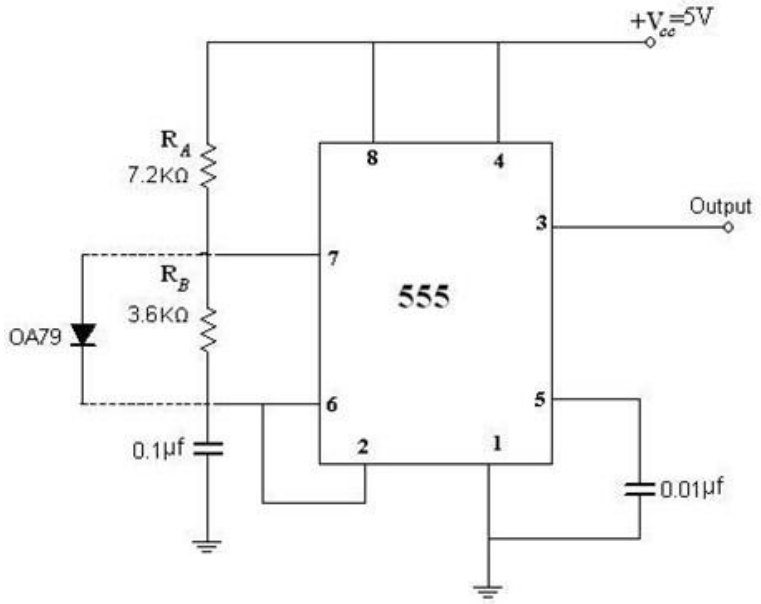
TABULAR COLUMN:

S.NO.	VOLTAGE (VOLTS)	CHARGING TIME T_C (SEC)	DISCHARGING TIME T_D (SEC)

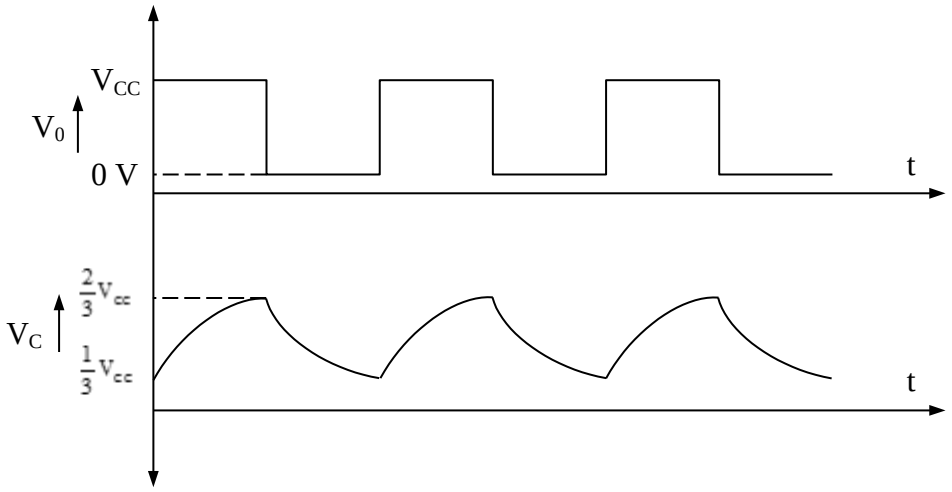
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the + Vcc terminal of the timer IC.
3. A negative trigger pulse of less than (1/3 VCC) i.e Ground to pin 2 of the 555 IC
4. At pin 3the output time period is observed with the help of a LED or CRO
5. At pin 6 the capacitor voltage is obtained in the CRO and the V0 and Vc voltage waveforms are plotted in a graph sheet.

b) ASTABLE MULTIVIBRATOR:



Model Graph:



DESIGN:

Given f= 4 KHz,

Therefore, Total time period, T = 1/f =

We know, duty cycle = tc /T

Therefore, tc =_____ and td = _____

We also know for an astable multivibrator, td = 0.69 (R2) C

Therefore, R2 = ----------

tc=0.69(R1+R2)C

Therefore,R1= ----------

TABULAR COLUMNS:

S.No.	VOLTAGE (VOLTS)	T_{ON} (mS)	T_{OFF} (mS)

S.No.	V_1 (VOLTS)	V_2 (VOLTS)	T_C (mS)	T_D (mS)

VIVA QUESTIONS:

1. What is a multivibrator?
2. What do you mean by monostable multivibrator?
3. Define duty cycle.
4. Mention the applications of IC 555.
5. What is a Schmitt trigger?

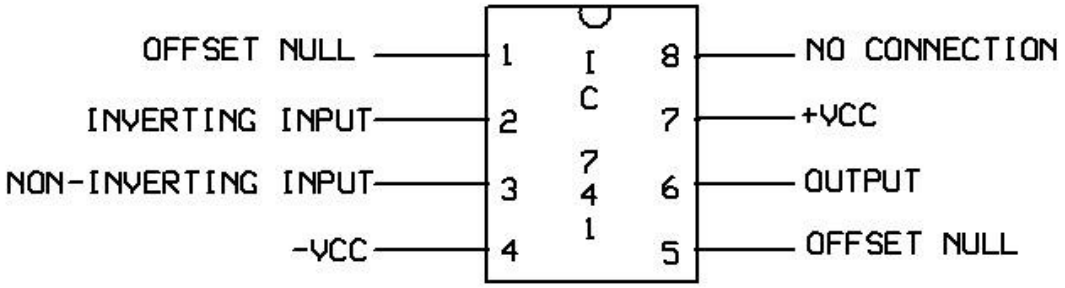
POST-LAB QUESTION:

1. The pulse width out of a one-shot multivibrator increases when the:
   a). supply voltage increases b). Timing resistor decreases
   c). UTP decreases d). Timing capacitance increases
2. The _____ is defined as the time the output is active divided by the total period of the output signal.
   a). on time b). Off time
   c). duty cycle d). Active ratio
3. The output of the astable circuit _____.
   a). constantly switches between two states
   b). is LOW until a trigger is received
   c). is HIGH until a trigger is received
   d). floats until triggered4.
4. If the resistor in the Schmitt trigger astable multivibrator is a variable resistor, which part of the output voltage waveform will change when the resistance is changed?
   a). the shape of the waveform b). The amplitude of the waveform
   c). the period of the waveform d). None of the above
5. The monostable multivibrator circuit is not an oscillator because _____.
   a). its output switches between two states
   b). it is not free-running
   c). it requires a sine wave input signal
   d). the circuit does not require a dc power supply

RESULT:

Thus the mono stable multi vibrator and astable multi vibrator using 555 timer for the given time period was designed and waveforms are obtained.

PIN DIAGRAM:



a). INVERTING AMPLIFIER:

DESIGN:

INVERTING AMPLIFIER: To design an amplifier for the gain of -10. Gain = R_f/R_1.As the Gain is given negative, the circuit is inverting amplifier. Gain Av = R_f/R_1 = 10 => R_f= 10 R_1. Let R_1= 1k, R_f = 10 * R_1 = 10 * 1k = 10k.

NON - INVERTING AMPLIFIER: To design an amplifier for the gain of 11.Gain = 1+ R_f/R_1.As the Gain is given positive, the circuit is non-inverting amplifier.Gain Av = 1+R_f/R_1 = 11 => R_f = 10 R_1. Let R_1= 1k, R_f = 10 * R_1 = 10 * 1k = 10k. **THEORY**:

INVERTING AMPLIFIER: A typical inverting amplifier with input resistor $R_1$and a feedback resistor R_f is shown in the figure. Since the op-amp is assumed to be an ideal one the input bias current is zero and hence the non -inverting input terminal is at ground potential. The voltage at node 'A' is Zero, as the non inverting input terminal is grounded. The nodal equation by KCL at node 'A' is given by V_i/R_1 + Vo/R_f =0 or V_0 = -R_f (V_i/R_1).

NON- INVERTING AMPLIFIER: A typical non-inverting amplifier with input resistor R_1 and a feedback resistor R_f is shown in the figure. The input voltage is given to the positive terminal. The output voltage is given by V_0= (1+R_f /R_1) Vi

DIFFERENTIAL AMPLIFIER: Basic differential amplifier is shown in figure, it amplifies the difference between the two input signal applied. The differential amplifier is characterized by the common mode rejection ratio (CMRR), which is the ratio of differential gain to common mode gain. The output voltage is given by V_0 = (R_2 / R_1) ($V_1 - V_2$), where V_1 and V_2 are the input voltages.

t_{low} = 0.25ms = 0.693R_b C;

Let C= 0.1µF => R_b = 0.25/(0.693X0.1X10^{-6}) =

t_{high} = 0.693(R_a + R_b)C = 0.75 ms => R_a =

i. For Symmetrical Wave form :

t_{high} = 0.693 R_a C; t_{low} = 0.693 R_bC

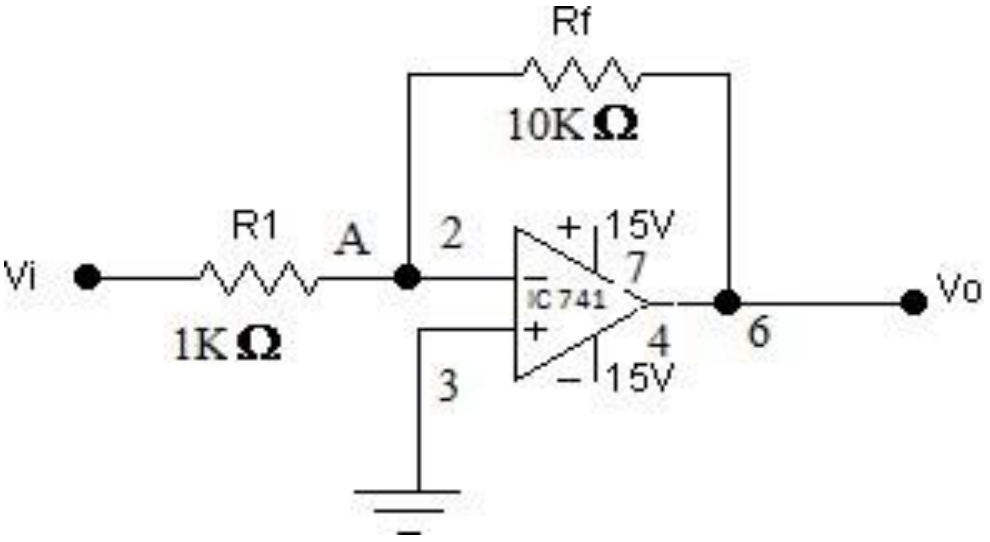
f = 1/T = 1.44 /(R_a + R_b)C => D= R_b /(R_a + R_b);

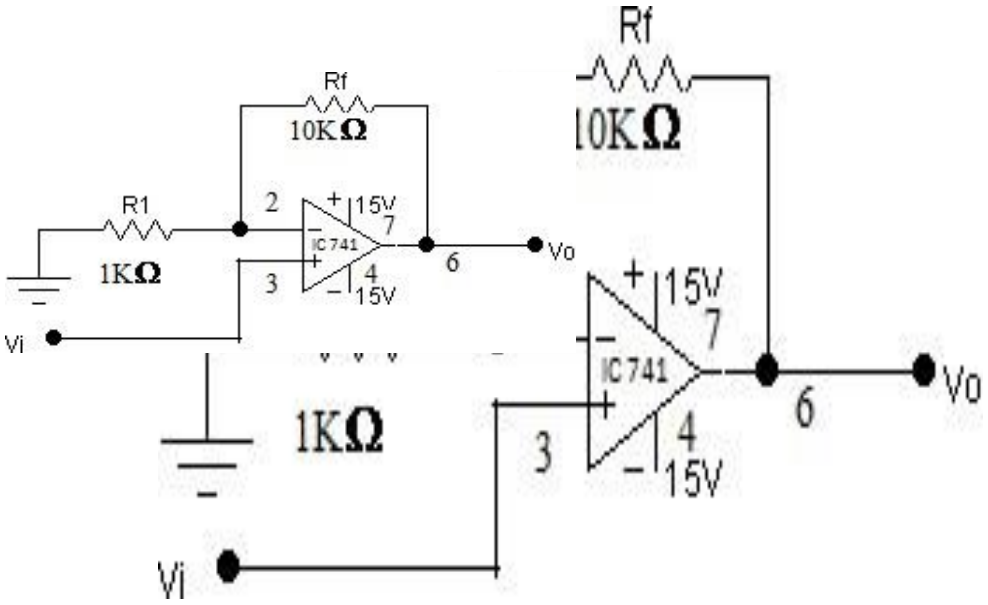
Specifications: frequency = 1 kHz; Duty cycle = 50% .Design: t_{low} = 0.5 ms = 0.693 R_bC;

Let C= 0.1 µF; R_b =

t_{high} = 0.693 R_a C = 0.5 ms ; R_a =

CIRCUIT DIAGRAM:





Ex. No. 9	APPLICATIONS OF OP-AMP
Date:	

INTRODUCTION:

Inverting Amplifier:

The fundamental component of any analog computer is the operational amplifier or op-amp and the frequency configuration in which it is used as an inverting amplifier. An input voltage V_{in} is applied to the input voltage. It receives and inverts its polarity producing an output voltage. This same output voltage is also applied to a feedback resistor R_f, which is connected to the amplifier input analog with R1. The amplifier itself has a very high voltage gain.

Non- Inverting Amplifier:

Although the standard op-amp configuration is as an inverting amplifier, there are some applications where such inversion is not wanted. However, we cannot just switch the inverting and non-inverting inputs to the amplifier itself.

Summing Amplifier

The Summing Amplifier is a very flexible circuit based upon the standard Inverting Operational Amplifier configuration. We saw previously that the inverting amplifier has a single input signal applied to the inverting input terminal.

Differentiator:

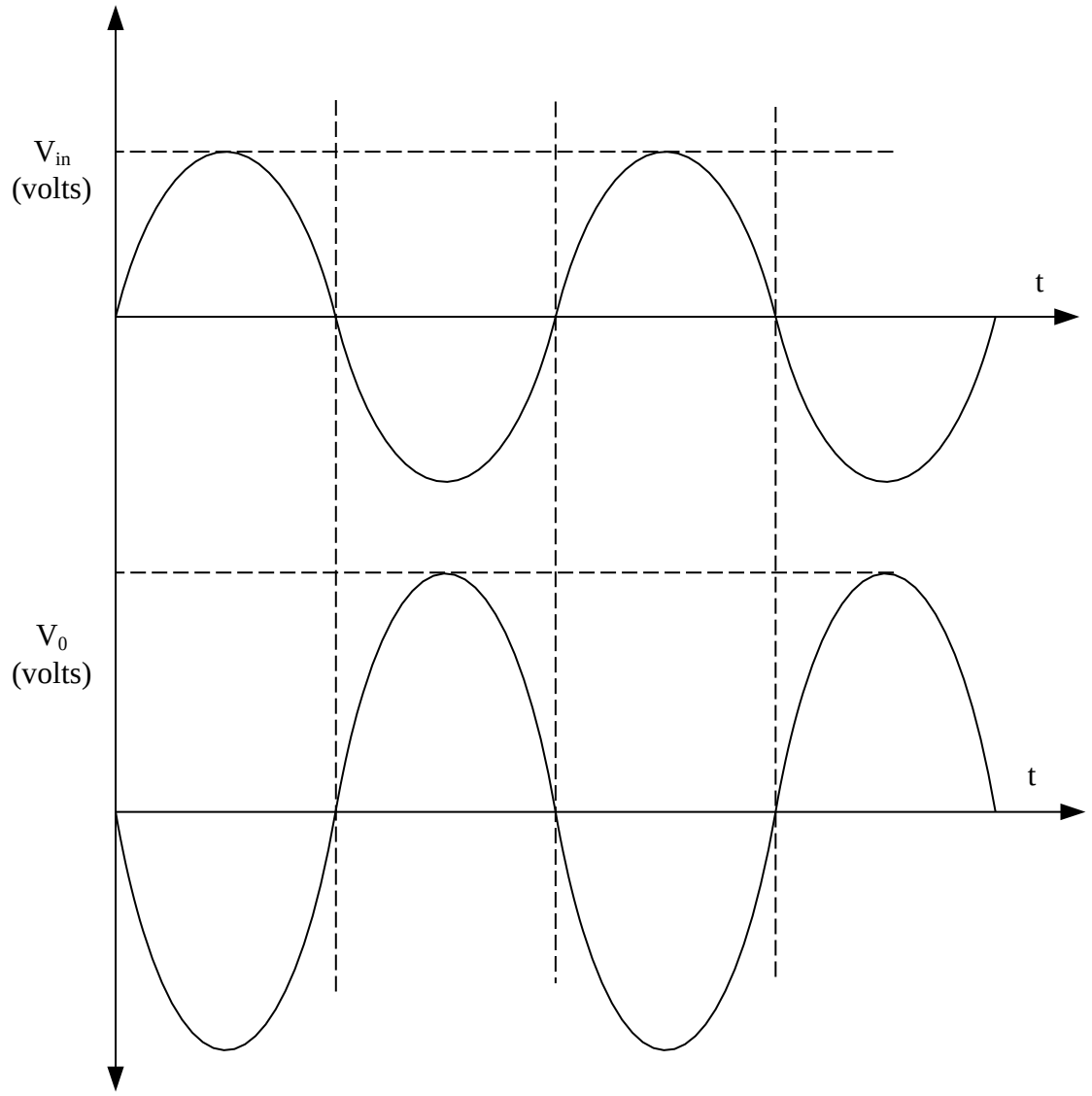
Op-amps allow us to make nearly perfect integrators such as the practical integrator the circuit incorporates a large resistor in parallel with the feedback capacitor. This is necessary because real op-amps have a small current flowing at their input terminals called the "bias current". The feedback resistor gives a path for the bias current to flow. The effect of the resistor on the response is negligible at all but the lowest frequencies. **Integrator:**

One of the simplest of the operational amplifier that contains capacitor is differential amplifier. As the suggests, the circuit performs the mathematical operation of differentiation. The output is the derivative of the given input signal voltage. The minus sign indicates a 180^0 phase shift of the output waveform Vo with respect to the input signal.

ANNA UNIVERSITY QUESTIONS

1. Design and verify the experimental and theoretical loop gains of amplifiers using IC 741 in the inverting and non-inverting modes. (50)
2. Design a circuit and study the operation of 741 op-amp as comparator. (50)
3. Design a circuit to study the operation of 1) Differentiator 2) Integrator. 3) Inverting summing amplifier. (100)
4. Design an inverting and non-inverting amplifier for a gain of 5 using operational amplifier IC 741. (100)
5. Design an integrator and a differentiator circuit using op-amp IC 741. Assume the input waveform to be sine waveform and square waveform. (100)

MODEL GRAPH:



AIM:

(a) To design and test the operation of inverting amplifier.

(b) To design and test the operation of Non-inverting amplifier.

(c) To design and test the operation of summing amplifier.

(d) To design and test the operation of Integrator.

(e) To design and test the operation of Differentiator.

(f) To design and test the operation of Comparator.

PRE-LAB QUESTIONS

1. The propagation delay of op-amp circuits can be tested using

   a). Differentiator b). LPF

   c). Comparator d). Difference amplifier

2. If the input to a comparator is a sine wave, the output is a

   a). Ramp voltage b). Sine wave

   c). Rectangular wave d). Sawtooth wave

3. A triangular-wave oscillator can consist of an op-amp comparator, followed by

   a). Differentiator b). Amplifier

   c). Integrator d). Multivibrator

4. The ramp voltage at the output of an op-amp integrator

   a). increase or decrease at linear rate b). Increases or decreases exponentially

   c). Always increasing d). Constant

5. Which devices can be used in place of the input and feedback resistors?

   a). Capacitors b). Inductors

   c). Diodes d). Light bulb

APPARATUS REQUIRED:

S.No.	Name of the Item	Range	Qty
1	IC 741		1
2	Resistors	1M·,1k·,10K·,100·,2.5K·,5.2K·	2
3	Capacitors	0.01· F,0.005· F	2
4	Dual Power Supply		1
5	RPS		1
6	Function Generator		1
7	CRO		1
8	Bread Board		1

9	Connecting Wires		

DESIGN:

$V_o/R_f = -(V_{in}/R_1)$

Then, $V_0 = -(R_f/R_1)*V_{IN}$

$R_{comp} \cdot R_{in}R_f / R_{in} \cdot R_f$

Let R_{in}=1kΩ, R_f=1MΩ

R_{comp}= 1kΩ

TABULAR COLUMN:

DC INPUT:

V_{in} (VOLTS)	**THEORETICAL OUTPUT (VOLTS)**	**PRACTICAL OUTPUT (VOLTS)**

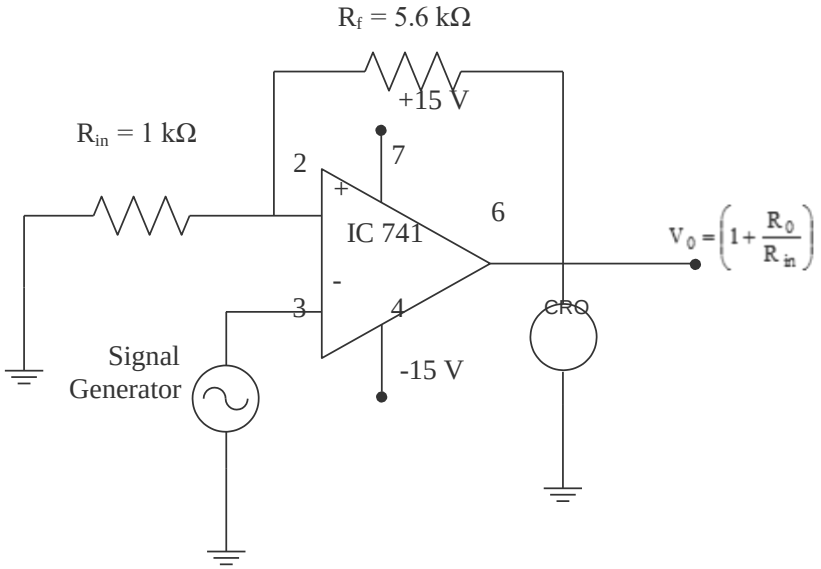
AC INPUT:

V_{in} (VOLTS)	**T_{in} (ms)**	**V_0 (VOLTS)**	**T_0 (ms)**

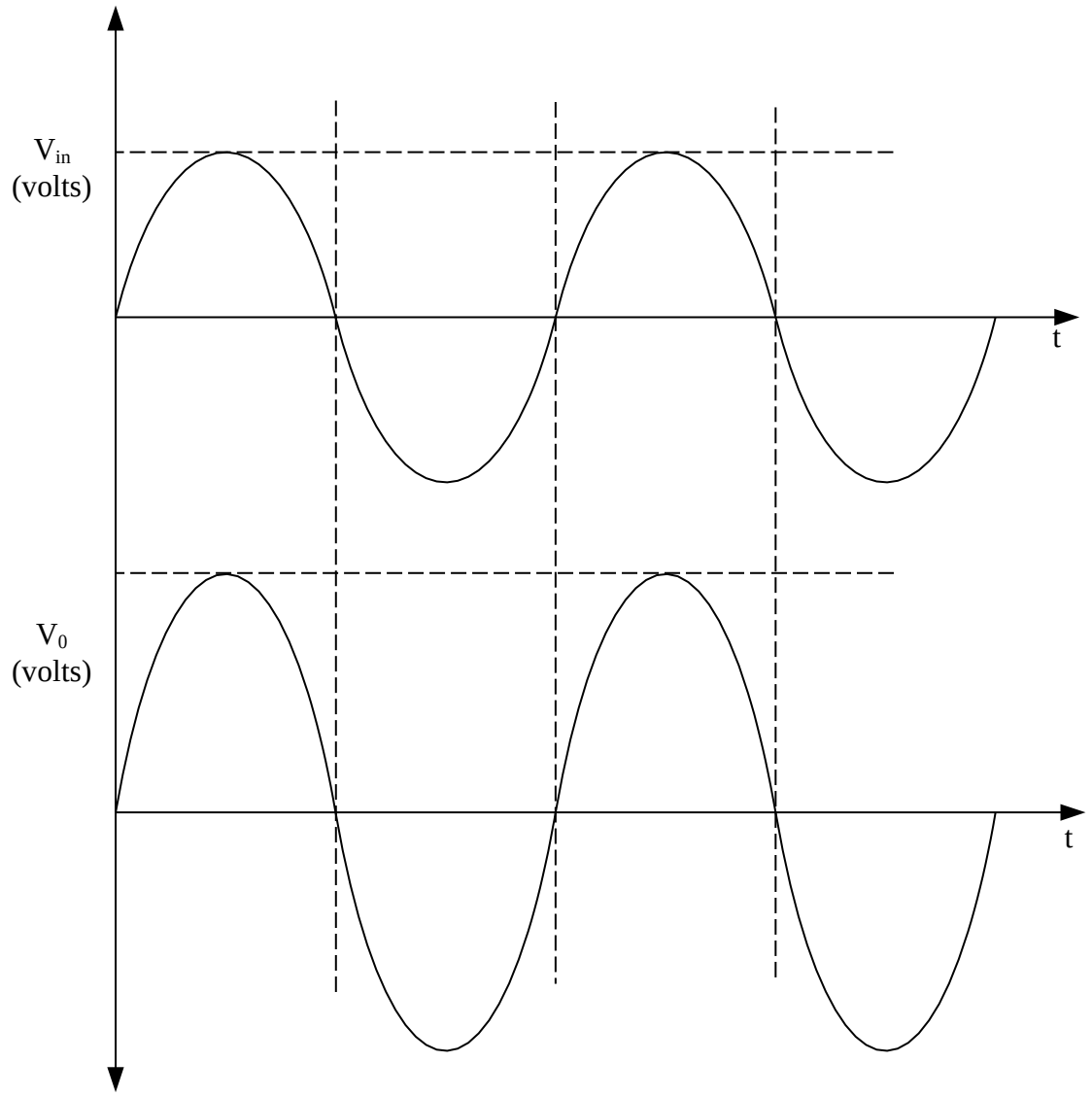
PROCEDURE:

1. The connections are made as per the circuit diagram.
2. The inputs are given and the outputs are observed from CRO.
3. In case of slew rate the input sine wave signal is adjusted so that the output is in peak time wave of 1 KHz, the frequency of the input is then increased until the output is diminished.
4. In case of comparator, the reference voltage V_{ref} is varied and the corresponding change in the waveforms are observed.

CIRCUIT DIAGRAM:



MODEL GRAPH:



b) NON INVERTING AMPLIFIER:

DESIGN

$V_0 = (1+ R_f/R_1)*V_{IN}$

R_{comp} · $R_{in}R_f$ / R_{in} · R_f

Let R_{in}=1kΩ, R_f=5.6 kΩ

TABULAR COLUMN:

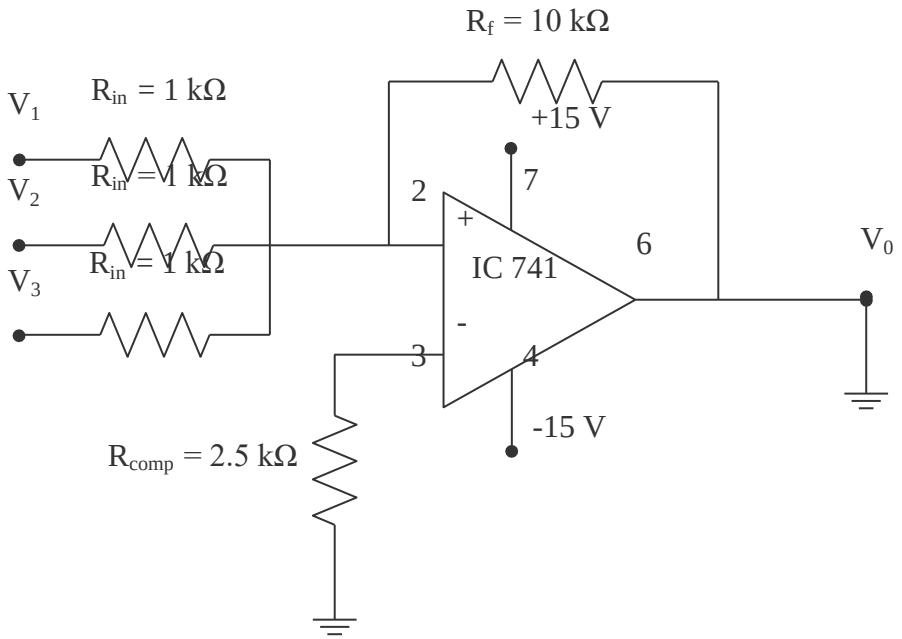
DC INPUT:

V_{in} (VOLTS)	**THEORETICAL OUTPUT (VOLTS)**	**PRACTICAL OUTPUT (VOLTS)**

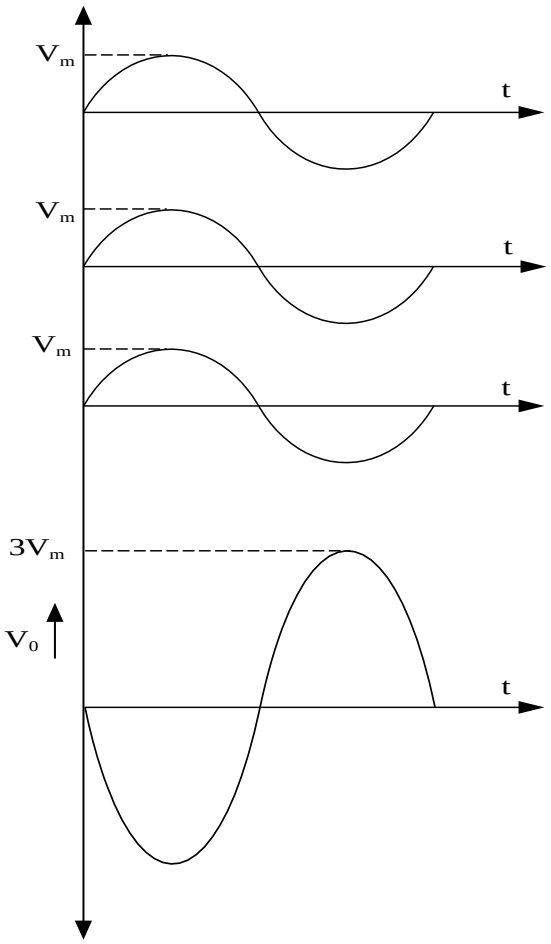
AC INPUT:

V_{in} (VOLTS)	**T_{in} (ms)**	**V_0 (VOLTS)**	**T_0 (ms)**

ADDER-CIRCUIT DIAGRAM:



MODEL GRAPH



c) ADDER:

DESIGN:

$V_o/R_f = -[V_1/R_1 + V_2/R_2 + V_3/R_3]$

If $R_1 = R_2 = R_3 = R_f$

Then $Vo = -[V_1 + V_2 + V_3]$ and

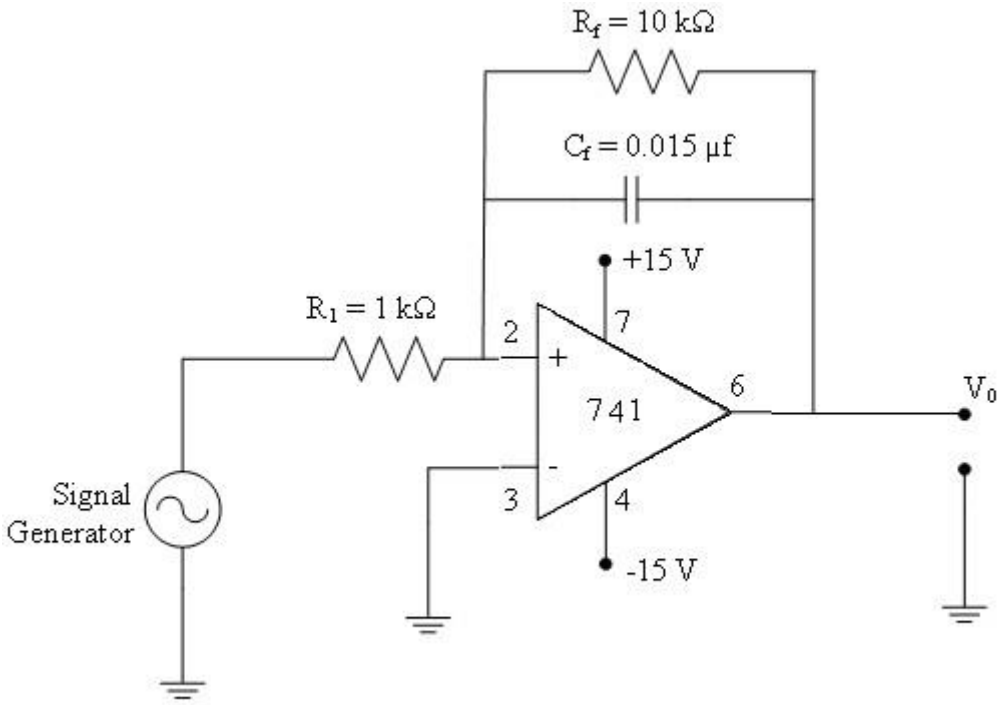
$Rcomp = R_1 \| R_2 \| R_3 \| R_f$

If $R_1 = R_2 = R_3 = R_f = 10$ K· ,then R comp =2.5 K·

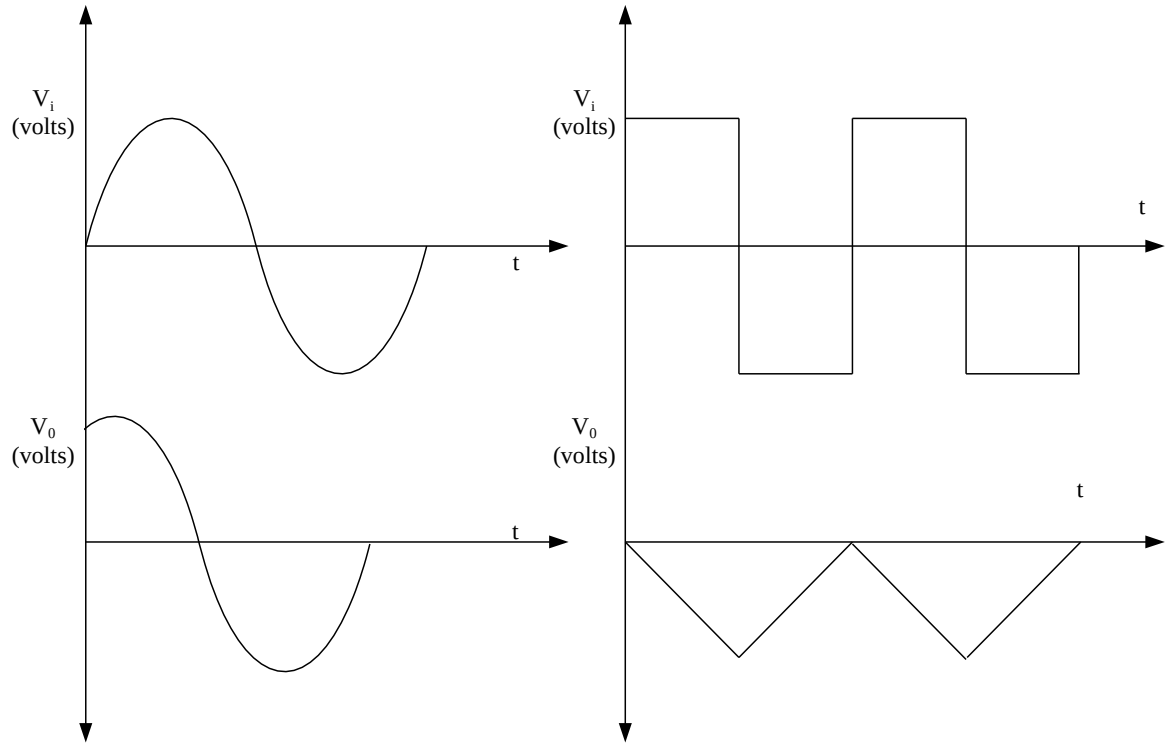
TABULAR COLUMN:

Wave form	**Amplitude (v)**	**Time (mS)**
Sine I/P O/P		

INTEGRATOR -CIRCUIT DIAGRAM:



MODEL GRAPH:



d) INTEGRATOR:

DESIGN:

In an integrator circuit, $F_a = F_b/10$ where Fa is the frequency of the periodic signal and F_b is the break frequency, assuming the values F_a= 1khz, R_f=10K· , F_b= 10Khz, R_1 = 1 K·

From which

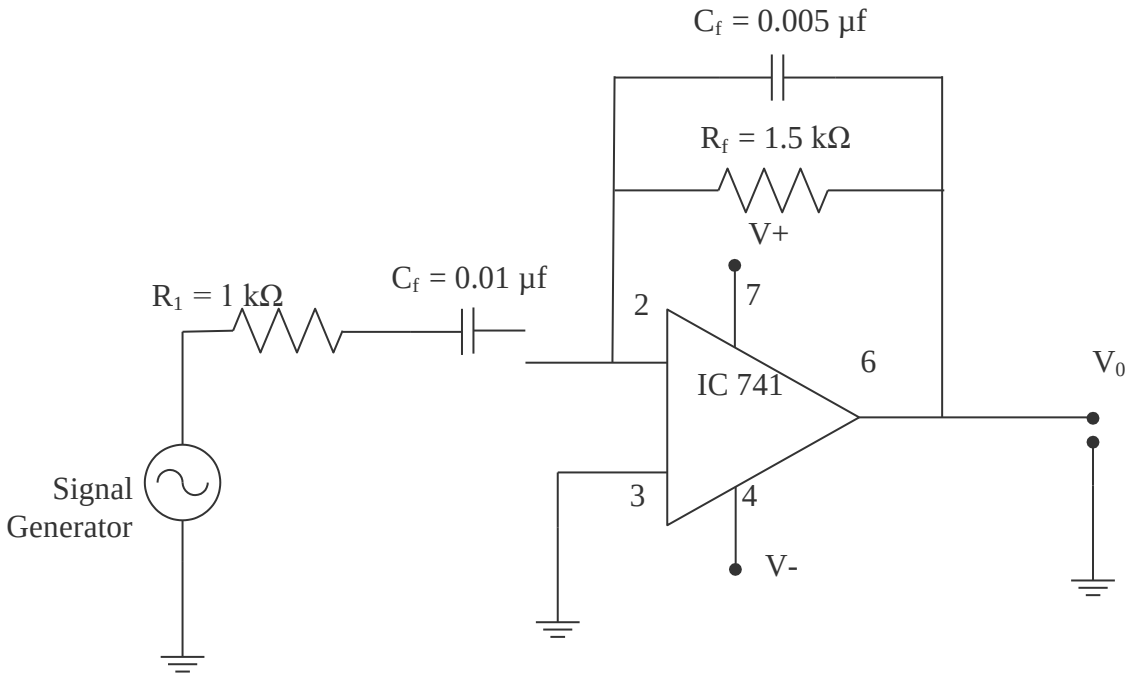
$F_a=1/ (2 · R_f C_f) = C_f = 1/(2 · R_1 F_a) => C_f = 0.015· f$

$F_b = 1(2 · R_1 C_f)= R_1 = 1(2 · F_b C_f) => R_1 = 1.06K·$

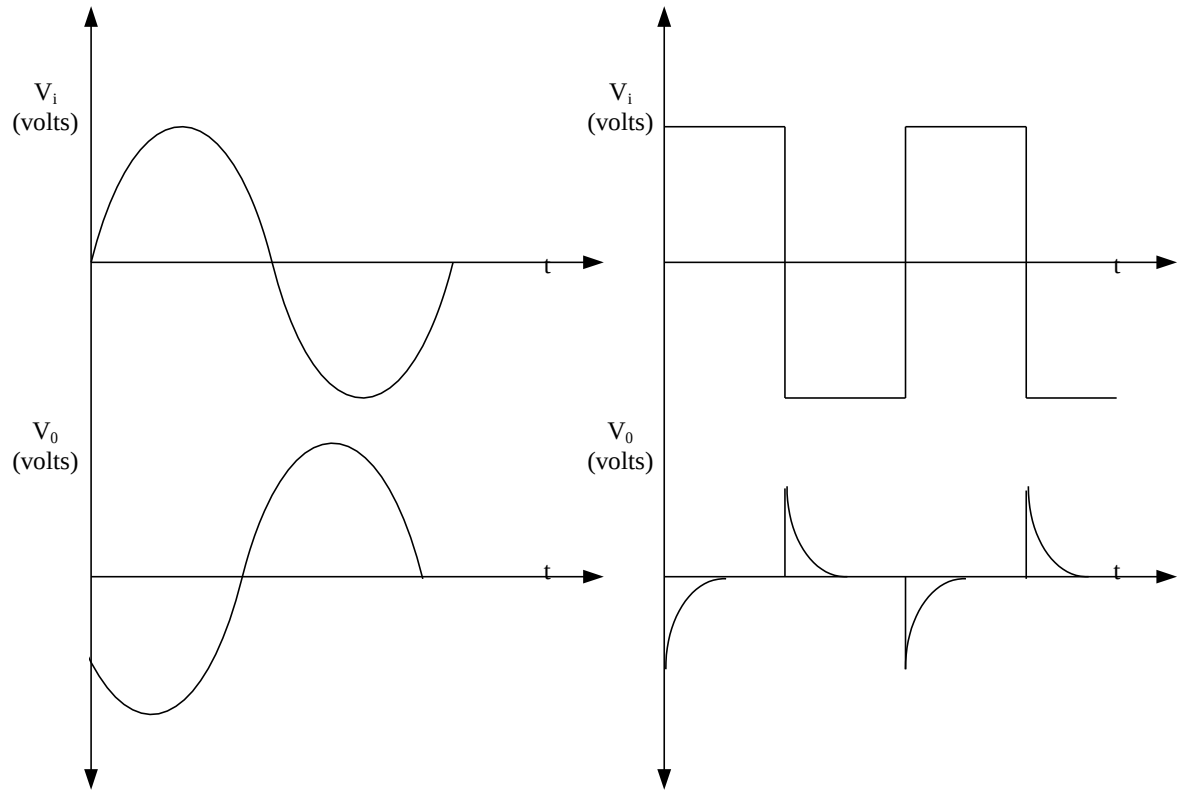
TABULAR COLUMN:

Wave form	**Amplitude (v)**	**Time (mS)**
Sine I/P		
O/P		
Square I/P		
O/P		

DIFFERENTIATOR -CIRCUIT DIAGRAM:



MODEL GRAPH:



e) DIFFERENTIATOR:

DESIGN:

F_b=20 F_a, selecting C_1 =0.1 · F (C<1· F) and F_a = 1KHZ then F_b= 20KHZ

From which

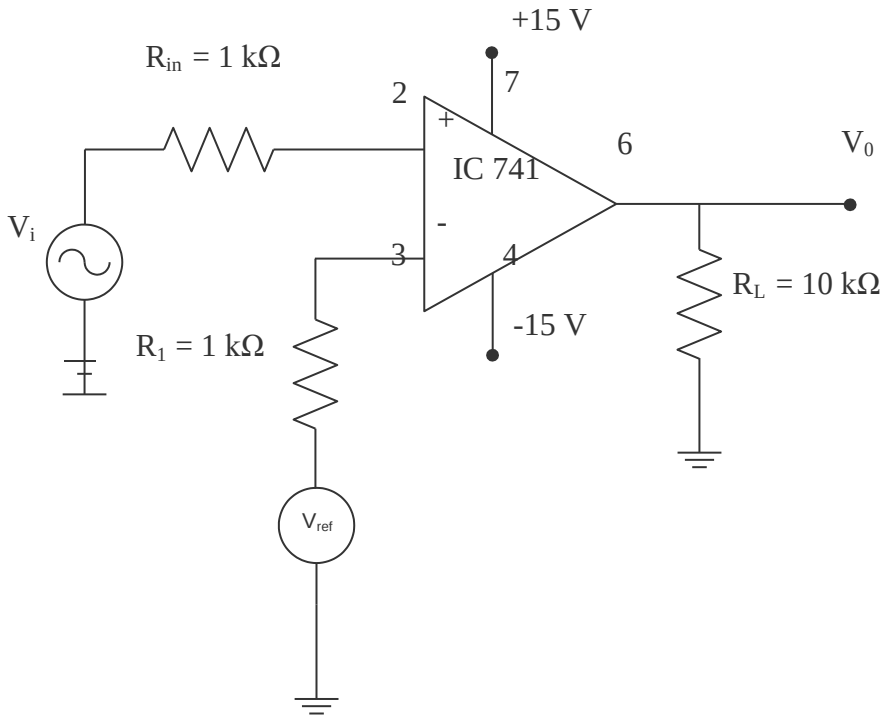
F_a = 1/(2 · R_f C_1) = R_f = 1/(2 · F_a C_1) = R_f= 1.5 K·

F_b = 1(2 · R_f C_f) = C_f = 1/(2 · F_b R_f) = C_f= 0.005· F

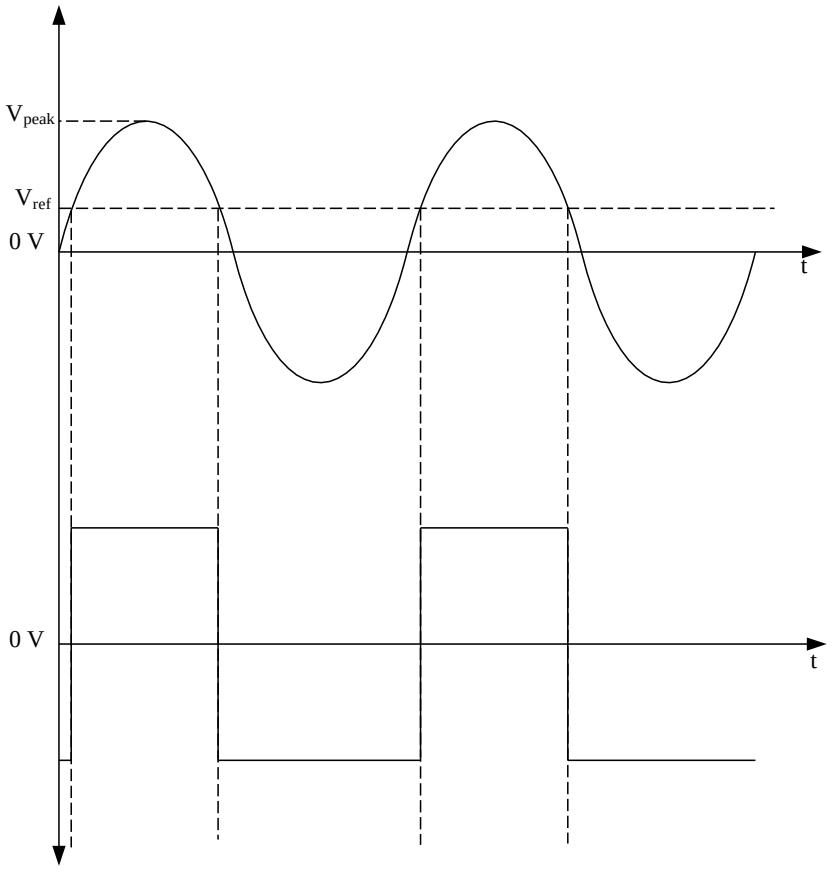
TABULAR COLUMN:

Wave form	**Amplitude(v)**	**Time (mS)**
Sine I/P O/P Square I/P O/P		

COMPARATOR -CIRCUIT DIAGRAM:



MODEL GRAPH:



f) COMPARATOR:

TABULAR COLUMN:

Wave form	Amplitude(v)	Time (mS)
Sine I/P O/P		

VIVA QUESTIONS:

1. Define an operational amplifier.
2. Mention the characteristics of an ideal op-amp.
3. Define input offset voltage.
4. Define input offset current.
5. What are the applications of comparator?

POST - LAB QUESTIONS:

1. Op-amp is a:

   a). Voltage-controlled voltage source (VCVS)

   b). Voltage-controlled current source (VCCS)

   c). Current-controlled voltage source (CCVS)

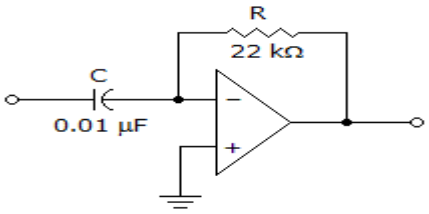
   d). Current-controlled current source (CCCS)

2. A comparator is an example of a(n)

   a). active filter b). current source

   c). linear circuit d). nonlinear circuit

3. Refer to the given figure. This circuit is known as



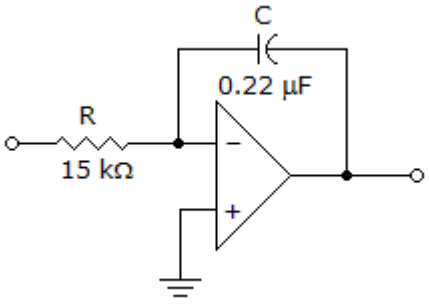
   a). a noninverting amplifier.

   b). a differentiator

   c) an integrator

   d) a summing amplifier

4. Refer to the given figure. A square-wave input is applied to this amplifier. The output voltage is most likely to be



   a). a square wave. b). a triangle wave.

   c) a sine wave d) no output.

5. In a(n) _____, when the input voltage exceeds a specified reference voltage, the output changes state.

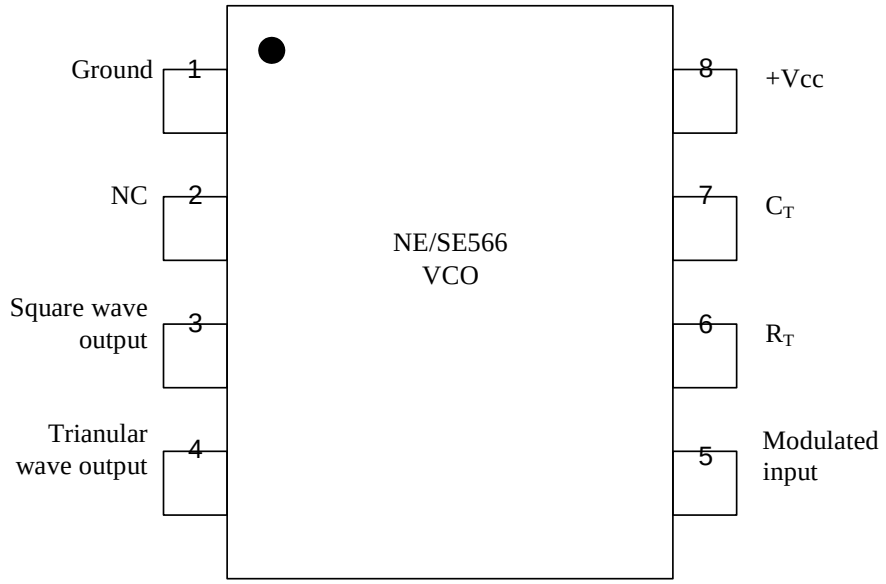
   a) integrator b) differentiator

   c) summing amplifier d) comparator

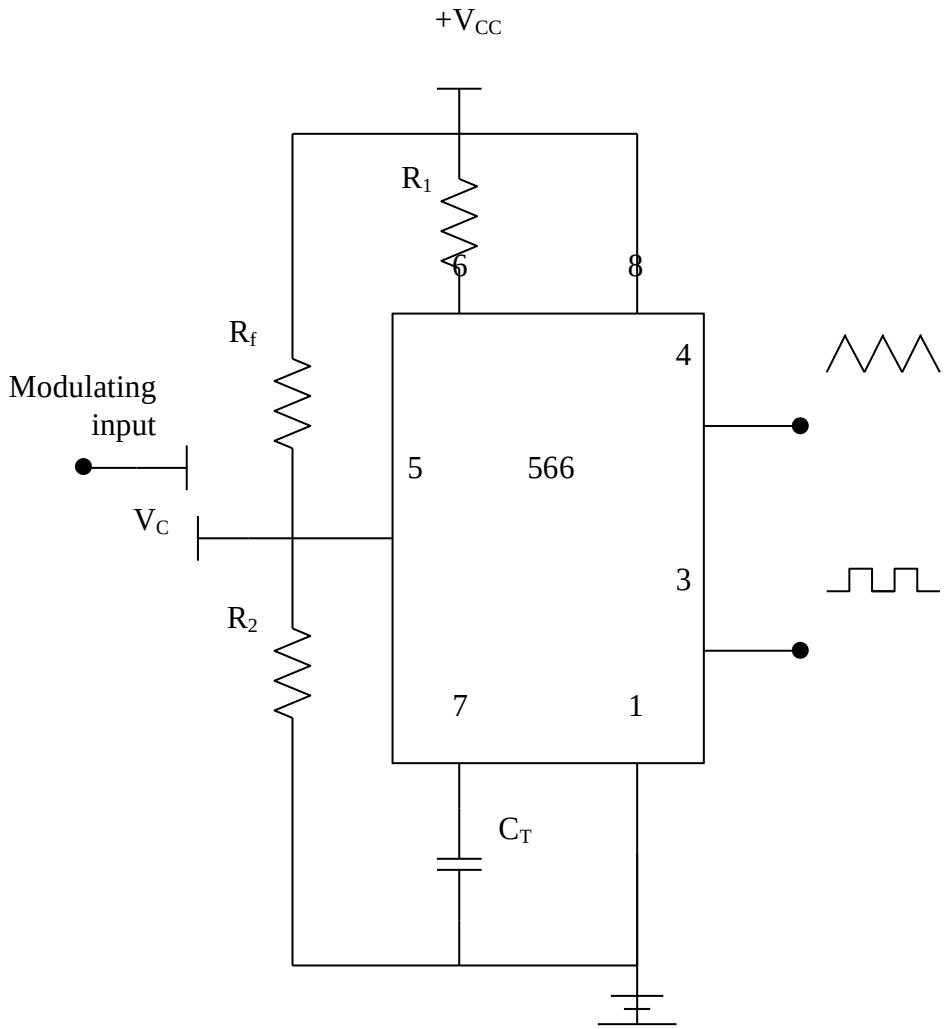
RESULT:

Thus the characteristics and applications of Op-Amp IC 741were verified.

PIN DIAGRAM:



CIRCUIT DIAGRAM:



Ex. No. 10	STUDY OF VCO AND PLL ICs
Date:	

VOLTAGE CONTROLLED OSCILLATOR:

A common type of VCO available in IC form as NE/SE 566. It consists of a timing capacitor C_T linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage V_c applied at the modulating input (Pin 5) or by changing the timing resistor R_r external to the IC chip. The voltage at Pin 6 is held at the same voltage as Pin 5. Thus, if the modulating voltage at Pin 5 is measured, the voltage at Pin6 also increases, resulting in less voltage across R and thereby decreasing the changing current.

The voltage across the capacitor C_T is applied at the inverting input terminal of Schmitt trigger A_2 via buffer amplifier. The output voltage swing of the Schmitt trigger is designed to V_{cc} and $0.5V_{cc}$. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting terminal of A2 swings from $0.5V_{cc}$ to $0.25\ V_{cc}$. When the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging the output of the Schmitt trigger goes low (0-5) $V_{cc.}$ The capacitor now discharges and when it is at $0.25V_{cc}$ the output of Schmitt trigger goes high.

MONOLITHIC PHASE LOCKED LOOP:

All the different building blocks of the PLL are available as independent IC packages and can be externally interconnected to make a PLL. Moreover a number of manufacturers have introduced monolithic PLL's too.

Some of the important monolithic PLL's are SE/NE 560 series introduced by signetics and LM560 series by rational semiconductor. The SE/NE 560,561, 562,564,565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. SE/NE 565 is the most commonly used PLL.

ANNA UNIVERSITY QUESTIONS

1. Construct a circuit to study the operation of NE565 PLL and to use it as frequency multiplier. (100)
2. Realize the voltage to frequency characteristics of 566 IC. (100)
3. Realize the frequency multiplication using NE/ SE 565 PLL IC. (100)

AIM:

(a) To study about voltage controlled oscillator.

(b) To study about Phase locked loop.

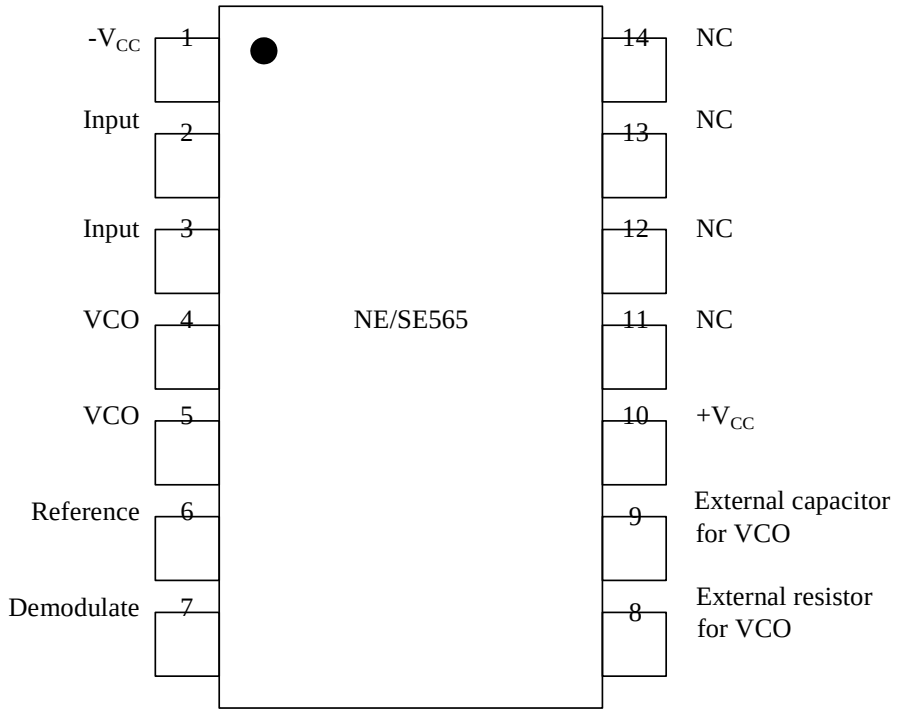
PRE-LAB QUESTIONS:

1. PLL consists of
   a). Phase detector b). VCO
   c). Phase defector d). All the above
2. VCO is designed so that at zero voltage it is oscillating at some initial frequency W_0 called
   a). cut-off frequency b). Free-cycle frequency
   c). free-running frequency d). None
3. The time takes for a PLL to capture the incoming signal is called
   a). Pull out time b). Capture time
   c). Lock out time d). None
4. The operating voltage of range of IC 565 is
   a). ±6 V to ±12 V b). ± 10 to ± 12 V
   c). ± 8 to ± 12 V d). ±12 V
5. _____ filter controls the capture range and lock range of PLL
   a). LPF b). HPF
   c). BPF d). None

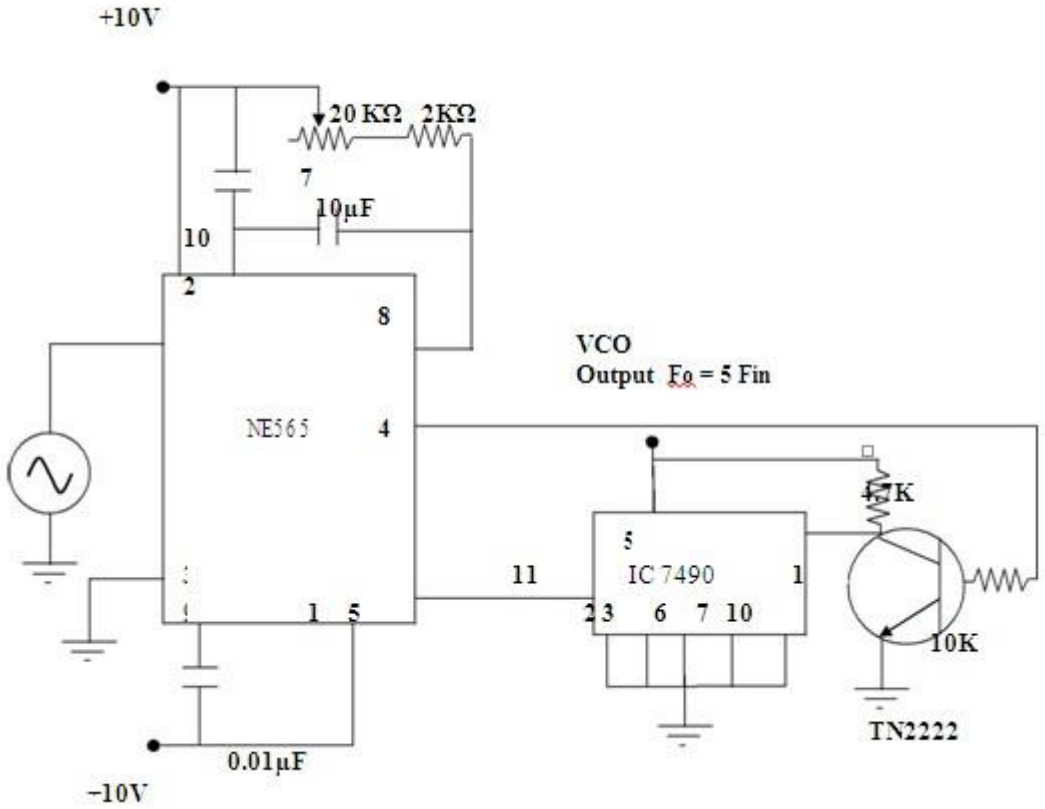
APPARATUS REQUIRED:

S.NO	COMPONENT	RANGE	QUANTITY
1	Digital IC trainer		1
2	PLL	NE565	1
3	VCO	NE566	1
4	Decade Counter	IC 7490	1
5	Resistor	2K, 4.7K,10K	3
6	Capacitor	0.001μF, 0.01μF, 10μF	3
7	Signal Generator	1	
8	POT	20K	1
9	RPS	(0-30V)	1
10	Connecting wires and probes		As required

PIN DIAGRAM:



CIRCUIT DIAGRAM:



The source and sink currents are equal, capacitor charges and discharges for, the same amount of the time.

Thus $\Delta v = 0.25V_{cc}$

$$\frac{\Delta V}{t} = \frac{i}{C_T}$$

$$\frac{0.25V_{CC}}{t} = \frac{i}{C_T}$$

$$t = \frac{0.25V_{CC} C_T}{i}$$

The frequency of oscillator f_0 is

$$f_0 = 1/t$$

$$= 1/2\Delta t$$

$$= \frac{i}{0.5V_{CC} C_T}$$

$$i = \frac{V_{CC} - V_C}{R_t}$$

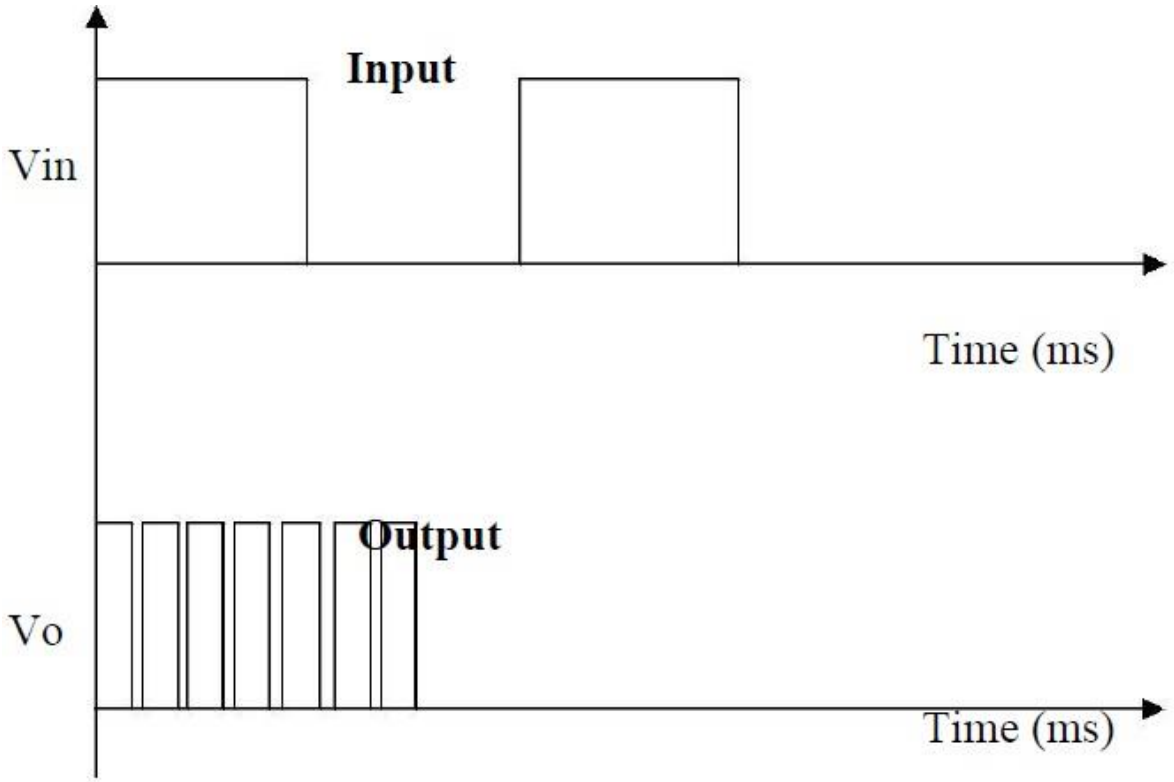
b) PHASE LOCKED LOOP:

To use PLL as a multiplier make connections as shown in fig the circuit uses and bit binary counter 7490 used as a divide by 5 circuit. Set the lip signal at 1 Vpp square wave at 500 HZ vary the VCO frequency by adjusting the by adjusting the 20k potentiometer till the PLL is locked Measure the output frequency it should be 5 times the input frequency repeat steps for input frequency of 1 KHZ

Fo=1.2/4R1 C1

It may be seen that phase locked loop is internally broken between the VCO output and the phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator, so as to compare f_0 with input signal f_s. A capacitor C is connected between Pin 7 and Pin 10 to make a low pass filter with internal resistance of 3.6KΩ.

WAVEFORMS:



VIVA QUESTIONS:

1. Mention some areas where PLL is widely used.
2. List the basic building blocks of PLL.
3. What are the three stages through which PLL operates?
4. Define lock-in range of a PLL.
5. What is meant by Capture range?

POST-LAB QUESTION:

1. What is the purpose of a sample-and-hold circuit?
   A. To keep temporary memory
   B. To hold a voltage constant so an ADC has time to produce an output
   C. To hold a voltage constant so a DAC has time to produce an output
   D. To hold data after a multiplexer has selected an output
2. Why are the maximum value of VOL and the minimum value of VOH used to determine the noise margin rather than the typical values for these parameters?
   A. These are worst-case conditions. B. These are normal conditions.
   C. These are best-case conditions. D. It doesn't matter what values are used.
3. In a frequency counter, what happens at high frequencies when the sampling interval is too long?
   A. The counter works fine. B. counter undercounts the frequency.
   C. The measurement is less precise. D. The counter overflows.
4. In the digital clock project, when does the PM indicator go high?
   A. Never
   B. Going from 11:59:59 to 12:00:00
   C. Going from 12:59:59 to 01:00:00
   D. On the falling edge of the clock after enable goes high
5. How is the output frequency related to the sampling interval of a frequency counter?
   A. Directly with the sampling interval
   B. Inversely with the sampling interval
   C. More precision with longer sampling interval
   D. Less precision with longer sampling interval

RESULT:

Thus the voltage controlled oscillator and the phase locked loop were studied.